

NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Computer Science and Engineering - NOC:Hardware Modeling using Verilog

Subject Co-ordinator - Prof. Indranil Sengupta

Co-ordinating Institute - IIT - Kharagpur

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1
Lecture 2
Lecture 3
Lecture 4
Lecture 5
Lecture 6 - Verilog Language Features - Part 1
Lecture 7 - Verilog Language Features - Part 2
Lecture 8 - Verilog Language Features - Part 3
Lecture 9 - Verilog Operators
Lecture 10 - Verilog Modeling Examples
Lecture 11 - Verilog Modeling Examples (Continued...)
Lecture 12 - Verilog Description Styles
Lecture 13 - Procedural Assignment
Lecture 14 - Procedural Assignment (Continued...)
Lecture 15 - Procedural Assignment (Examples)
Lecture 16 - Blocking / Non-Blocking Assignments - Part 1
Lecture 17 - Blocking / Non-Blocking Assignments - Part 2
Lecture 18 - Blocking / Non-Blocking Assignments - Part 3
Lecture 19 - Blocking / Non-Blocking Assignments - Part 4
Lecture 20 - User Defined Primitives
Lecture 21 - Verilog Test Bench
Lecture 22 - Writing Verilog Test Benches
Lecture 23 - Modeling Finite State Machines
Lecture 24 - Modeling Finite State Machines (Continued...)
Lecture 25 - Datapath And Controller Design - Part 1
Lecture 26 - Datapath And Controller Design - Part 2
Lecture 27 - Datapath And Controller Design - Part 3
Lecture 28 - Synthesizable Verilog
Lecture 29 - Some Recommended Practices

Get Digi-MAT (Digital Media Access Terminal) For High-Speed Video Streaming of NPTEL and Educational Video Courses in LAN

www.digimat.in

NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

- Lecture 30 - Modeling Memory
- Lecture 31 - Modeling Register Banks
- Lecture 32 - Basic Pipelining Concepts
- Lecture 33 - Pipeline Modeling - Part 1
- Lecture 34 - Pipeline Modeling - Part 2
- Lecture 35 - Switch Level Modeling - Part 1
- Lecture 36 - Switch Level Modeling - Part 2
- Lecture 37 - Pipeline Implementation Of A Processor - Part 1
- Lecture 38 - Pipeline Implementation Of A Processor - Part 2
- Lecture 39 - Pipeline Implementation Of A Processor - Part 3
- Lecture 40 - Verilog Modeling Of The Processor - Part 1
- Lecture 41 - Verilog Modeling Of The Processor - Part 2