

## NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Computer Science and Engineering - Design Verification and Test of Digital VLSI Circuits

Subject Co-ordinator - Dr. Santosh Biswas, Prof. Jatindra Kumar Deka

Co-ordinating Institute - IIT - Guwahati

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Introduction to Digital VLSI Design Flow

Lecture 2 - High Level Design Representation

Lecture 3 - Transformations for High Level Synthesis

Lecture 4 - Introduction to HLS

Lecture 5 - Scheduling Algorithms - 1

Lecture 6 - Scheduling Algorithms - 2

Lecture 7 - Binding and Allocation Algorithms

Lecture 8 - Two level Boolean Logic Synthesis - 1

Lecture 9 - Two level Boolean Logic Synthesis - 2

Lecture 10 - Two level Boolean Logic Synthesis - 3

Lecture 11 - Heuristic Minimization of Two-Level Circuits

Lecture 12 - Finite State Machine Synthesis

Lecture 13 - Multilevel Implementation

Lecture 14 - Introduction to formal methods for design verification

Lecture 15 - Temporal Logic

Lecture 16 - Syntax and Semantics of CTL

Lecture 17 - Syntax and Semantics of CTL â Continued

Lecture 18 - Equivalence between CTL Formulas

Lecture 19 - Introduction to Model Checking

Lecture 20 - Model Checking Algorithms - I

Lecture 21 - Model Checking Algorithms - II

Lecture 22 - Model Checking with Fairness

Lecture 23 - Binary Decision Diagram

Lecture 24 - Ordered Binary Decision Diagram

Lecture 25 - Operation on Ordered Binary Decision Diagram

Lecture 26 - Ordered Binary Decision Diagram for State Transition Systems

Lecture 27 - Symbolic Model Checking

Lecture 28 - Introduction to Digital VLSI Testing

Lecture 29 - Functional and Structural Testing

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## NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

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- Lecture 30 - Fault Equivalence
- Lecture 31 - Fault Simulation - 1
- Lecture 32 - Fault Simulation - 2
- Lecture 33 - Fault Simulation - 3
- Lecture 34 - Testability Measures (SCOAP)
- Lecture 35 - Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras
- Lecture 36 - D-Algorithm - 1
- Lecture 37 - D-Algorithm - 2
- Lecture 38 - ATPG for Synchronous Sequential Circuits
- Lecture 39 - Scan Chain based Sequential Circuit Testing - 1
- Lecture 40 - Scan Chain based Sequential Circuit Testing - 2
- Lecture 41 - Built in Self Test - 1
- Lecture 42 - Built in Self Test - 2
- Lecture 43 - Memory Testing - 1
- Lecture 44 - Memory Testing - 2