CHARGING INFRASTRUCTURE

Prof. Apurv Kumar Yadav

Department of Electrical Engineering

Indian Institute of Technology Roorkee

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Lecture-8

Lec 08: Revisiting Diode Bridge Rectifier with Capacitive Filter - II

Hello everyone, welcome to this lecture number 8. of NPTEL lecture on charging infrastructure here in the previous lecture we were revisiting some of the concept of diode bridge rectifier with capacitive filter we will continue our discussion. In this particular lecture as well in this we were discussing that we have the full bridge rectifier where we have four diodes connected in a fashion as shown over here and in this particular thing we can able to source power to the load in both the positive half cycle and negative half cycle we were trying to size this particular converter. Since we have only capacitor here and the four diodes we are we were trying to derive or we were trying to see what will be the value of capacitance and how that value of capacitor determines different ratings of these diodes as well. So, we were seeing the operation of this particular converter. This particular diode is rectified with capacitive filter where we have seen that in positive half cycle, it is the D1 and D4 who will be in conduction while in negative half cycle is D2 and D3 which will be in conduction.

And if you see only during that means the output voltage 'v_d' will be varying between the $v_{d,max}$ and $v_{d,min}$ and using this particular this capacitive filter we can able to restrict the output voltage or variation of output voltage within a certain band which is within a certain limits which is between $v_{d,max}$ and $v_{d,min}$ and that particular $v_{d,max}$ and $v_{d,min}$ would be one of the specification which will say that the output ripple in the converter should be within this particular voltage range. And in this we have seen that whenever the input voltage v_s in the, let us say in the positive half cycle becomes greater than this $v_{d,min}$, then only the D1 and D4 gets forward biased and that is when the current will be drawn from the source, current will be drawn from

the source as shown over here between or the point where the input voltage becomes greater than the $v_{d,min}$. And then it continues until where the AC input reaches to its peak value. And after that point, the input voltage will drop down.

However, the capacitor will keep holding that particular voltage. And we see that the current going into the capacitor will be there between t_a to t_b instance. that means the current will be drawn from the source only between t_a to t_b instant and this difference of t_a and t_b. We will define it as a t_c which is nothing but the time during which the capacitor gets charged. However in the remaining period the capacitor will be discharging until in the next half cycle the input voltage the magnitude of input voltage will become greater than the '$v_{d,min}$ at that particular point in the negative half cycle it's the D2 and D3 which gets forward bias and then it will get it will i mean the current will be drawn from the source and that's when the capacitor gets charged up from '$v_{d,min}$'to '$v_{d,max}$'and this '$v_{d,max}$',whenever or the voltage or the input voltage whenever it reaches the peak value at that point again the D2 and D3 gets reverse bias and that is when again there will not be any current drawn from the source and it's the capacitor which will be which will be giving giving power to the load and that's when its voltage gets discharged to a value will mean here we see during this instance it's the D1 and D4 which is in conduction always get forward bias and will allow the current to flow through it and during this period it's the D2 and D3 which is getting forward bias and the current will be drawn from the source. Similarly, we have also derived the capacitance value which is actually nothing but $(1 - t_c/(\frac{T}{2}))$. where T is the time period corresponding to the input frequency which is 50 Hz or input AC frequency which is 50 Hz and 'P_L' which is again the load power or the power which has to be delivered to the load, V_0which is the nominal value of the output nominal value of the output voltage whereas the ΔV_0 is the voltage ripple which is again nothing but ($v_{d,max} + v_{d,min})/2$.

$$V_0 = \frac{V_{d\,max} + V_{d\,min}}{2}$$

$$\Delta V_0 = (v_{d,max} - v_{d,min})$$

So, in order to keep the output voltage ripple within the permissible limit one need to size the capacitor accordingly and this t_c one can also define this time period during which you want the capacitor to get charge so this is one t_c is the one value which is dependent upon the value which the designer can select to appropriately size its component. So, these are the things we discussed in the last class.

Now, let us see we have derived the value of capacitance. However, the size of the capacitor bank which is there or the size of the capacitor which is there in the capacitive filter depends upon the voltage it is blocking, as well as obviously the capacitance value which we have derived and also depends upon the how much rms value of current which is going through this capacitor so let us derive those which will help you to design the capacitor bank if you are using the full bridge based rectifier with capacitive filter for your ac to dc conversion. So, let us define some of the constraint or the points such as or some of the variables in this circuit so let us first take the variable I_L which we have already also defined in this figure. So 'I_L' is the one which is actually the average value of this 'i_d' current.

However, the remaining portion of the current will be flowing through this capacitor C. So, 'I_L' is nothing but the average value of the current which will be or the average value of the 'i_d' current which is coming out of the diode bridge rectifier. So now this 'I_L' value we can define it as simply the P_L value the load power divided by the average value of voltage average value of the voltage at the output.

$$I_L = \frac{P_L}{V_o}$$

So, this average value which is nothing but $(v_{d,max} + v_{d,min})/2$ as we have shown is nothing but our V_O value so that we can define that is the average value of the 'i_d' current now. Similarly, now this average value of the ideal current, if we see the ideal current, this is the ideal current variation and let us assume this ideal current to be a square wave. So, if we assume the ideal current to be a square wave like this, this is the assumption we have taken, a simpler assumption.

To reach to a conclusion because defining this variation is quite difficult so we can take the assumption which is we assume that the current is nothing but a kind of a fixed it is drawing $i_{s,pk}$ value between 't_a' to 't_b' that means for 't_c' duration it is drawing '$i_{s,pk}$', current and then it becomes to zero it is slightly this this assumption is slightly on a conservative sense so that even if we select our capacitor for the required or capacitor for the required rms current we will not be undersizing the capacitor bank so this assumption is in the conservative sense. So, as we have taken this as assumption, now let us since we have considered our assumption to be, I mean the idle current to be drawing a fixed $i_{c,pk}$ value during 't_c' duration. So, the 'I_L' value will be average of this particular current. So, this we can write also this 'I_L' as nothing but $i_{s,pk}$ the average value we can write it for 't_c' duration there for 't_c' duration during the time period $T/2$ during this period for this for $T/2$ period because it repeats after every $T/2$ period this 'i_d' current. So, the average value of that 'i_d' will be $i_{s,pk}$ t_c divided $T/2$ which is nothing but equal to I_L.

$$I_L = i_{s,pk} \times \frac{t_c}{T/2}$$

Now this particular from these two particular equations we can write down that $i_{s,pk}$ is nothing but $T/2$ t_c* PL divided V_o is peak at $T/2$ t_c P_L multiplied by 2 divided by $v_{d,max,}$ plus $v_{d,min}$.

$$i_{s,pk} = \frac{P_L}{V_o} \times \frac{t_c}{T/2}$$

$$i_{s,pk} = \frac{2P_L}{(v_{d,max} + v_{d,min})} \times \frac{t_c}{T/2}$$

Now, if you look very carefully this in this particular expression of $i_{s,pk}$ which is which we obtain in this in this particular which we obtain here. Now, if we look very carefully this $i_{s,pk}$ is inversely proportional to 't_c'. That means whenever we want this $v_{d,max,}$ to be closer to $v_{d,min}$ that means delta V_o to be nearly equal to 0 that is when we are making this duration from this 't_a' to 't_b'

duration to goes to 0 that means the 't_c' value goes to 0 and thus when we are making the tc value goes to 0 in we are making sure this $i_{s,pk}$ goes to infinity. So, thus we can from this particular expression we can expect that if this $v_{d,max}$ is becoming very much nearer to $v_{d,min}$ that implies my 't_c' is going slowly towards zero or we can instead of writing this we can also write the 't_c' is going towards zero and that's when the $i_{s,pk}$ value goes towards infinity or you can say that very high value.

So, thus this is a drawback of this particular capacitor filter: if we want to ensure the ripple between $v_{d,max,}$ and $v_{d,min}$ is as small as possible. Or the ripple in the output voltage to be as small as possible. That is when we are ensuring, or making, the time duration for which the capacitor gets charged as small as possible. That is when we are making the current drawn from this source a very high current for a very small period of time. So, this is one of the drawbacks of this particular system.

Now, let us see how, using this particular assumption that the current drawn from the source is nearly constant (equal to the $i_{s,pk}$) during the 't_c' duration. How we can calculate, or using this particular assumption, let us see how we can calculate the RMS current going through the capacitor C. So, let us see how we can calculate the current through the capacitor. Now, considering the same waveform we have drawn previously, let us understand how we can draw the current through the capacitor. Now, if you look carefully, it is during this period—from this point to this point—that the capacitor will be supplying the load. That means if I draw it, the capacitor will be delivering to the load or discharging into the load. In this period—that is, in a $T/2$ period—it is only during this point to this point that it is discharging, while during this tc period it is charging. So, we can write here: the capacitor is charging, and here: the capacitor is discharging.

Its energy into the load. So, let us see how we can write the RMS current through the capacitor. Again, the assumption is the same: the current drawn from the source— Or the 'i_d' will be in the manner drawn in the green-colored waveform. That's the assumption we have taken. So, during the tc period, if you look carefully, during the 't_c' period, it's the current which is coming from

here. During the 't_c' period, the current coming from here is the current going through the capacitor as well as the current going through the load.

So, the current which is going through the capacitor, we can write down it as the RMS value. We can write down this as during 't_c' period the current through the capacitance we can write or the rms current through the capacitor we can write this since this is the constant $i_{s,pk}$ so $i_{s,pk}$ minus I_L which is the current average current which is going through the load that is the current remaining current will be flowing through the capacitor during the time 't_c' in a time over the time period $T/2$ because after $T/2$ it again repeats the current waveform or this idle current waveform repeat itself similarly during 't_c' minus $T/2$ period that means remaining of the $T/2$ period the 'i_c',rms will be nothing but because during this period during this remaining of the period it is a capacitor which will be discharging to the load that means providing power to the load that is when we can write this 'i_c',rms to be nothing but IL multiplied by 1 minus t_c divided $T/2$.

During 't_c' period,

$$i_{c,rms} = (i_{s,pk} - I_L) \times \sqrt{\left(1 - \frac{t_c}{T/2}\right)}$$

During '$t_c - T/2$' period,

$$i_{c,rms} = I_L \times \sqrt{\left(1 - \frac{t_c}{T/2}\right)}$$

That we can write and that's when the overall inner $T/2$ period we can write capacitor rms is nothing but nothing but $i_{s,pk}$ minus I_L square times t_c divided 2 plus I_L times 1 minus I_L square times 1 minus t_c divided $T/2$.

$$i_{c,rms} = \sqrt{\left(I_{s,pk} - I_L\right)^2 \times \frac{t_c}{T/2} + I_L^2\left(1 - \frac{t_c}{T/2}\right)}$$

So the overall 'i_c',rms will be given by this expression so thus for capacitor selection we know that the rating of capacitor if we see the voltage rating of capacitor voltage rating of capacitor is nothing but is nothing but whatever the average value of V_o we were getting plus delta V_o divided 2 which is nothing but equal to we can say that it's a $v_{s,pk}$ because it's a peak value to which it goes.

$$v_{s,pk} = V_0 + \frac{\Delta V_O}{2}$$

And we can also say that the capacitance value we have obtained as 1 minus t_c divided $T/2$ multiplied with $P_L/2$ times V_o ΔV_o multiplied with 1 divided f_s.

$$c = \left(1 - \frac{t_c}{T/2}\right) \times \frac{P_L}{2v_0\Delta v_0} \times \frac{1}{f_S}$$

And the RMS current rating which is RMS current rating is nothing but rms $i_{c,rms}$ as:

$$i_{c,rms} = \sqrt{\left(I_{s,pk} - I_L\right)^2 \times \frac{t_c}{T/2} + I_L^2\left(1 - \frac{t_c}{T/2}\right)}$$

And this rms current rating is important because this will actually determine the parallel combination of capacitance because the capacitance will have its own current rating so the capacitor bank must be in a position to handle this much 'i_c',rms current and this 'i_c',rms current it depends on the $i_{s,pk}$ the load current average load current obviously the 't_c" which is the designer's choice and $T/2$ which is nothing but t corresponds to 1 /50 Hz and accordingly one can calculate the 'i_c",rms and which will actually determine what will be the pair what parallel combination of capacitance is needed and if one is using parallel combination then also need to understand whether to connect that parallel combination with series capacitance or not so and also the voltage rating must be you know vsp or you can say that average value of output voltage plus half of the ripple which is nothing but equal to '$v_{d,max}$', itself it will come down to that only and capacitance value is calculated in this manner with these three considerations one can easily design a capacitor bank or capacitive filter for if they choose to select the full bridge direct rectifier with capacitor filter for their ac to dc power converter now let us also calculate if

you look very carefully along with this capacitor we also have the diode and we also have to define the rating of the diode for proper selection of the diodes so let us calculate the diode ratings different ratings of the diode so let me find the diode selection.

Now if we see the diode selection the first and foremost thing is obviously vrrm which is peak repetitive reverse voltage which is nothing but your $v_{s,pk}$ nothing but V_o plus delta V_o divided 2, that's the maximum voltage how we are calculating that's the maximum voltage.

$$v_{RRM}=v_{s,pk} = V_0 + \frac{\Delta V_o}{2}$$

So, if we consider this one the peak value of this will go up to $v_{s,pk}$ and when this is a $v_{s,pk}$. Let's say if the D4 is in conduction that's when is the D3 which will be blocking the entire V_o or entire voltage across it. So that's why this diode has to block that voltage which goes up to $v_{d,max}$'or you can say that $v_{s,pk}$'now I mean if you see very carefully it is during this period assume during this period is D1 and D4 is conducting so it's the D2 and D3 which will be blocking the voltage 'v_d' which is nothing but going from $v_{d,min}$'to $v_{d,max}$'across it. So, that's why the peak repetitive voltage is nothing but your $v_{s,pk}$ which we have written over here. And similarly, the peak forward current, so if we see the peak forward current.

If we see here, so in the positive half cycle, it's the D1 and D4 which will be carrying or which will be having this 'i_d' current. While in the negative half cycle, it's the D2 and D3 which will be carrying this 'i_d' current and it's the maximum value, its maximum value is nothing but the $i_{s,pk}$. That's when the peak forward current for all the D1, D2, D3, D4 is nothing but $i_{s,pk}$value current value so if we are trying to reduce the voltage ripple in the output capacitance that's when we will increase the capacitance value at the same time we will be reducing the time for which which is required to charge the capacitor that and also we will require a diode with the larger peak forward current because if we are making the $v_{d,max}$ and $v_{d,min}$ very much go up very much so the peak forward voltage is nothing but the highest peak and the if we try to calculate the average forward current diode forward current we try to see what will be the thing so again in our assumption which is that during 't_c' period it's the constant $i_{c,pk}$value which has

been drawn from the source that means the 'id' value is nothing but a constant $i_{c,pk}$ during tc period so during this period it's a D1 and D4 which will be conducting and that will repeat only after T duration only after one cycle in the next positive cycle it's the D1 and D4 will again conduct and similarly the D2 and D3 is conducting in a negative half cycle and only during in the next negative half cycle it will be conduct it will be in conduction. So that's when the average forward current forward is nothing but $i_{s,pk}$ times tc divided T, because it's in the time duration T.

$$\langle I_F \rangle (D1, D2, D3, D4) = i_{s,pk} \times \frac{t_c}{T}$$

where i mean during the time duration T the diode forward current for D1, D2,D3,D4 all the four diodes will be just 't_c' divided by T, because it is only for the t_c duration during one line cycle the diode is conducting and it will be carrying this $i_{s,pk}$ current because that's the assumption we have taken. Similarly, we can also calculate the rms Current going through the diode, again this is needed to calculate the I^2t rating. So, that we can calculate that is nothing but $i_{s,pk}$ times for the 't_c' duration it is conducting, root tc divided T it is conducting over the period time.

$$i_{rms} = i_{s,pk} \times \sqrt{\left(\frac{t_c}{T}\right)}$$

So, that is when we can calculate the RMS current rating of the diode using this particular method. One can select the diode for this full-bridge converter with a capacitive filter. These are the ratings used to select the diode. Let us see what the disadvantages of this converter are because understanding the disadvantages will motivate us to move to the next converter. The disadvantage is obviously the peaky current drawn from the source. That means the current drawn from the source is no longer sinusoidal. It is a peaky current, or you can say it is non-sinusoidal as well. That means it includes a lot of harmonics.

It will have a lot of harmonic content in it. So, this leads to peaky current drawn from the source. With this, the current drawn is at non-unity power factor. So, the current drawn is at non-unity power factor. This again violates one of the requirements of having this AC-to-DC converter for chargers. That means we always want to have unity power factor current drawn

from the source. This particular current, which is peaky in nature and obviously non-sinusoidal, introduces a lot of harmonics into the source. At the same time, it is at non-unity power factor. The next disadvantage is the oversizing of the components.

Let's say if we make sure our $v_{d,max}$ and $v_{d,min}$ are very close to each other. That's when we are making sure ΔV is nearly zero. That's when we can make tc nearly zero. That is when we can ensure that our C value, which we have calculated here, has increased. So, the capacitance value has increased. Also, if you look carefully, our RMS current ratings i_{rms} of the capacitor or $i_{c,rms}$ of the capacitor increases. Also, we will see that $i_{s,pk}$ value increases, which actually leads to an increase in the forward peak current. So, this will also lead to a significant oversizing of the component.

However, one of the advantage with this particular converter is the output voltage is nearly constant, you can say that varying within the permissible So, this is one advantage we get from this converter that in the previous converter where the output is continuously varying in the form of rectified sinusoidal DC. So, here we can avoid that and we can get the output voltage to be varying within our permissible limit. which was not the case previously where the voltage was going from 0 to the peak value and then coming back to 0.

So, in over the 2,3 going through this revisiting of 2,3 converters what we understood. Let us try to write down those understanding because that understanding is the one which will determine us to go ahead and understand why the next kind of converter is being used and how we can define or design that particular converter. So, what are the learnings we obtain? What are the learnings?

Let us write down the learnings in the process of revisiting the lectures. So, the first learning what we obtain is the unity power factor of the drawn current or of the source current can be achieved when the load is purely resistive power or you can say that the power is being delivered in both the positive and negative cycle in both positive and negative half cycles that is the first learning we obtain However, when doing this thing, we understood that the output voltage is not constant.

It varies between 0 to $v_{s,pk}$ and then again goes down to 0 in the rectified DC form. So, the next thing we understood is that the output voltage can be made nearly constant. or within a permissible limit, it can be made nearly constant by adding the output capacitor filter. However, if we do that, the current drawn will become non-sinusoidal and deviate significantly from the unity power factor. So, that is why

the next family of converters, or this will lead to another type of converter called a power factor correction converter, which is used to obtain unity power factor current drawn. along with. So, to obtain unity power factor current drawn along with regulated voltage, the power factor correction converter is used. Now, what is a power factor correction converter? So, let me draw the variation or the type of power factor correction converter.

So, in this, they will again take the full-bridge diode rectifier. And right after this diode bridge rectifier, they will place a power converter. and then add the output of this one, a capacitive filter supplying the load 'R_L'. Now, this power converter is made to operate in such a manner that the input impedance of this power converter will be purely resistive, and thus, this diode bridge rectifier will see a resistive load, drawing unity power factor current from the voltage source. Now, 'i_s' will vary in the same manner as 'v_s', maintaining unity power factor with no phase shift between 'v_s' and 'i_s'.

If by somehow, while doing the operation of this converter, we make sure that the input impedance seen by or the input impedance offered by this power converter because of its operation is such that it is having the resistive nature, and that's when the diode bridge rectifier will see the output as having the resistive load. That's when the current will be of the unity power factor, and since we are using a capacitance at the output, this capacitor will be used to keep the voltage or the output voltage within the permissible limit defined in the specification. So, we will see the different kinds of power converters we can have in the next class, and I hope we could have been able to understand how logically the power factor correction converter came into existence. We will discuss in detail in the next class the different kinds of power factor correction converters and their operation. Thank you.