CHARGING INFRASTRUCTURE

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Week-08

Lecture-38

Lec 38: Phase Shifted Full Bridge (PSFB) Converter-II

Hello everyone welcome to the lecture number 38 of this NPTEL lecture series on charging infrastructure and today we will discuss the second part of phase shifted full bridge converter methods and modulations i mean operations we were whatever we were discussing so we will discuss the second part of that if we recall in our previous lectures we have started discussing different modes where we saw first mode where S1 and S4 the diagonal switches were conducting Since they were conducting the is actually $V_{C4} = 0$, the V_{C3}voltage of the capacitor C3 is V_{in}, $V_{C1} = 0$, $V_{C1} = V_{in}$ then at $t = t_2$ we have removed the pulse from the S1 switch since we remove the pulse from S1 switch in order to ensure ip current to be still be there because which is nothing but the reflected current from the output load inductor what happens is that the current will start flowing through the capacitor in the top capacitor the current will be going into the capacitor that means it is charging the C1 capacitor in the bottom capacitor it is discharging the capacitor here the V_{C2} will be discharging from V_{in} to 0 and the C1 is actually charging from 0 voltage to some voltage and if we look very carefully the $V_{AB} = V_{C2}$ voltage and V_{C2} voltage since it is falling down it is discharging. So, it is discharging with the slope $\frac{I_1}{(C_1+C_2)}$ where $I_1$is nothing but the reflected current of the i_L and if we consider this to be nearly same as I_0 , so it is and I_0 we can just say that and since my V_{AB} is falling down the V_R voltage is also falling down in that same manner and here we can say I_P is nothing but IC1 to be nothing but I_P is nothing but equal to summation of I_{C1} and I_{C1} the current through the C1 and C2

capacitors. And from there, we have just calculated the voltage, which will be how the voltage will be appearing across the C1 capacitor, how the voltage which will be appearing across the C2 capacitor. And we saw that at the time period between t_1 to t_0 is nothing but $\frac{2CV_{in}}{I_1}$.

we got and after t_{01} that means at we can say $t = t_1$ what we see is that V_{C2} goes to 0 that means if the VC2 goes to 0 my diode can now turn on. So here at that point my diode turns on and in order the moment the diode turns on the voltage across this switch S2 will become 0 and then you can start giving the pulse to the S2 switch to achieve the turn on of this switch S2 with ZVS or 0 voltage.

Now here if you look very carefully , so before that S1 was on then you have turn off the S1 switch and S2 was already off so during that time there was a dead time i mean there is no active pulse given to both S1 and S2 , so and this that time if i can ensure this that $dead\ time > t_{01}$ time if we can ensure this $dead\ time > t_0$, one time then i can ensure that the switch S2 goes through ZVS turn on or you can say soft switching of this S2 will be achieved and same thing will also repeat uh after 180^0 or the after when when i mean after the S2 is off and when S1 is turning on. So we will achieve the same condition after the 180^0 ,we can say after $\frac{T_s}{2}$ period we will get the same kind of you know mechanism and we can say that for the leading leg switches the ZVS turn on is ensured if we can ensure that dead time greater than $\frac{2CV_{in}}{I_1}$.that means the time after which the S1 gate pulse turns off and S2 pulse is given you know S2 is given turn on pulse. then after that what happens we enter into the mode 3 where my S2 switch is on. So, in the leading lag I have already switch over from S1 switch to S2 switch now the condition comes when I have to go for the lagging switch. So, let's say after at T2 the S4 switch turns off because the S4 switch is turns off what happens is that the voltage across $V_{AB} = -V_{C4}$ and in $-V_{C4}$. Since V_{C4} is rising because of the current direction so we see that the voltage across this V_{AB} is going in the negative direction which is shown over here since the voltage is going in the negative direction the I_P will be falling and it will difficult for I_P to catch up with the reflected current of the output inductor and as a result of which the output indicator has to find a path to flow that's when DR1 and DR2 gets forward bias the moment the DR1 and DR2 gets forward bias the voltage across primary winding is zero and the entire vab will be appearing across the L_{lkg} and as a result of which what we will see is that this L_{lkg} will be resonating with C3 and C4 capacitor and that's when that resonance is there and that's when we have derived our V_{C4} voltage and V_{C3} voltages. Now we can say that at $t = t_3$, that means

when we reach at this point at $t = t_3$, we can say that the $t_2 = t_3$, we can say $t_2 - t_3$, at $t = t_3$, what happens is that at $t = t_3$, if you wanted to ensure that the capacitor voltage of a C3 goes to zero this C3 goes completely to zero that means the capacitor V_{C4} the voltage of V_{C4} has to go to V_{in} then only i can ensure my V_{C3} is completely discharged through this current i_p. So we can say that at t_3 if $V_{C3} = 0$ then we can say my V_{C4} goes to V_{in} and then we can write down my t_{23} to be nothing but equal to from here we can just calculate which is

$$t_{23} = \frac{1}{\omega_1} sin^{-1}\left(\frac{V_{in}\sqrt{\frac{2C}{L_{lkg}}}}{I_2}\right)$$

we will get our t_{23} value to be this one and the moment the voltage of V_{C3} goes to 0 the diode D3 the diode D3 will get turned on and if the diode D3 will get turned on, the voltage across S3 switch is equal to zero. And when the voltage across S3 is zero, you will give the turn on pulse to S3.

So, you will achieve the zero-voltage switching of the switch S3. So, this is where, you know, at $t = t_3$,, if we assume our V_{C3} goes to 0 and V_{C4} goes to V_{in}, so our t_{23} value will become something like this. Now comes the mode 4 where the S3 switch need to turned on after S4 switch turned off. So, we have to give the dead time. So, we can say the dead time period of lagging lag.

If I can ensure the dead time period of the lagging leg switches is greater than t_{23}that means we can say that dead time of lagging leg is greater than if we recall this thing is

$$dead\ time\ of\ lagging\ leg\ > \frac{1}{\omega_1} sin^{-1}\left(\frac{V_{in}\sqrt{2C}}{I_2}\right)$$

Now if this condition satisfies that means if the time after which the S3 switch turns on is greater than t_{23} that indicates the V_{C3} goes to zero and and that's when D3 turns on and switch S3 achieves zero voltage turn on for the leading leg it was you know we were getting a very simpler expression because there we have this L_{lkg} and L both are coming in the series in this case only the L_{lkg}part is there because on the secondary side in order to ensure the $i_L$current both the DR1 and DR2 is forward biased DR1 and DR2 is forward biased that's when they are forward

that's when the V_R voltage is still zero if you see over here it is still zero. So here what happens is that now your D3 is turned on and your S2 is already on.

So now what is happening is that across theV_{AB}, you are now have started applying minus V_{in} voltage. We are now applying minus V_{in} voltage. And here if you look very carefully, if you look very carefully, my V_{AB} is nothing but, you know, in the mode 3, if you look very carefully, the V_{AB} is nothing but minus V_{C4}. And since my V_{C4} is charging up, so the voltage is going towards V_{in} voltage. here we have drawn a straight line but it is not straight line it is having sinusoidal variation but for approximations we have drawn a straight line and similarly for i_p also there is slight sinusoidal variation same as that of V_{AB} variation.

So now what we have seen is that the voltage of this V_{AB} was V_{C3} in the previous mode 3 case in mode 4 case the V_{AB} is now since my D3 is on., so minus $-V_{in}$ voltage is started appearing across the across the V_{AB} since the $-V_{in}$ voltage is appearing across the V_{AB} the current i_p will be falling in you know will be falling from you know it previously it was i_L then it went to I_2 from I_2 at this point it is falling you know linearly because you are applying minus V_{in}voltage across V_{AB} and since my i_p is very very much smaller than this i_L. So, this DR1 and DR2 is forward bias in order to ensure the inductor current has the continuity so what we understood in case of leading lag switches, we have to provide dead time greater than t_{01} in order to ensure the soft switching of S1 and S2 switch. In the lagging lag switches, in order to ensure the dead time, we must ensure the dead time of the lagging lags to be equal to t_{23}. And during the t_{23} period, it is the L_{lkg} which is actually resonating with the C3 and C4 and so the current which is flowing through the L_{lkg} must have that much energy to discharge the C3 capacitor to zero and that's when turning on the diode D3 and charging the capacitor C4 to v in voltage So, we will see that necessity condition as we go, you know, at last we will see. But during this time, we assume that if we are having the, you know, soft switching, we must provide at that time. So, this is nothing but this is the that time of lagging switch. Lagging lag.

Here that time of leading lag. So, what we are getting is we got this V_{in}, you know, here V_{in} is there and this V_{in} is appearing across this. And since this i_p is no longer equal to i_L, this DR1,

DR2 is forward bias. That's when you will see zero voltage which is appearing across here. And this V_{AB} will only be appearing across this L_{lkg}.

And this because of this thing, this i_L which is there is falling linearly. And this they will fall linearly with the slope $\frac{-V_{in}}{L_{lkg}}$. why because your DR1 and DR2 is forward but that's when that's when the secondary winding is fully short circuited since secondary one is fully short circuited this at the voltage at this point is nearly zero the vab is actually appearing across the only across the L_{lkg} and we know that the $V_{AB} = -V_{in}$,so this will be appearing across the L_{lkg} case so during this mode 4 case. We can write this $i_p(t)$. we can say you know it is falling from some non-zero value at this value this point. So, let us say this is me

$$i_p(t_3) = \frac{-V_{in}}{L_{lkg}}(t - t_3)$$

So, from this point from this point to this point is a straight line so we can just write this particular expression and we know that at and this continue until i_p reaches to 0 at $t = t_4$ further in this during this duration we can also provide if you look very carefully after the that time which is greater than t_{23}, period we are also giving the gate pulse to S3 switch as well so now my S3 switch is now on so what is happening is that during that time we can say that at we can say at t equal to t_4.

At $t = t_4$., at this particular point, what we will see is that the your $i_p(t_4)$=0, that is when we can say that

$$t_{43} = t_4 - t_3 = L_{lkg}\frac{i_p(t_3)}{V_{in}}$$

so this is the time of t_{43} and if we recall between t_{23} our time was this t_{23} and if we do the previous case between t_{12} if we take the between. So in during the t_{01} we have this period and in t_{12}, t_{12} is nothing but you know the delta period which you are providing. You know the delta phase shift which you are providing.

So now let us see what is happening at $t = t_4$, at $t = t_4$ my current which is going is actually going and reaching to zero point since my current is reaching to zero point and my S3 switch is on what happens is that from $V_{AB} \approx -V_{in}$ voltage is applied and so you know so what happens the i_p will keep on growing again this minus is you know this $-V_{in}$ voltage is coming over here This $-V_{in}$ voltage is coming over here. Since it is already short circuited, the voltage across this is zero. So this voltage is coming across this point at T4.

And this continues until, you know, from this point, this i_p current will keep on going. Will keep on going from here. It goes to this point and then coming back like this. It keeps on going in a negative direction. And during this point, my $V_{AB} = -V_{in}$ and S3 is now on.

S2 is already on. So and since this thing is there, the i_L current in order to ensure i_L current is maintained, the DR1 and DR2 is forward bias. DR1 and DR2 is forward bias. biased and we can say i_L can be write as,

$$i_L = i_{DR1} + i_{DR2}$$

Since both are conducting secondary short circuited at this point it is short circuit at this point from here to here it is zero and the entire $V_{AB} = -V_{in}$ is actually $-V_{in}$ coming across a leakage coming across a leakage Since my S3 is already on, so I do not need to bother about the time during which this thing continues.

So, this we can say during this time between t_4 to t_5, again my current is actually kept on going, going, going in the negative direction until it becomes equal to i_L current and that is when my DR1 ceases to conduct and in the entire, you know, DR2 will start conducting. So, let us try to find the expression for this thing. So, here the winding voltage is 0. Still the winding voltage is equals to 0. So, the entire V_{AB} is imposing upon this L_{lkg}.

So, we can write down that

$$i_p(t) = \frac{-V_{in}}{L_{lkg}}.$$

So, this slope is nothing but $\frac{-V_{in}}{L_{lkg}}$. the slope is going on t minus t_4 which we are having and that's when we can say at $t = t_5$, it keeps on going, going, going. And until the point when this at this point at $t = t_5$, I can say $i_p(t_5)$ is nothing but the reflected current from the inductor in the negative direction.

$$i_p = -ni_L$$

So, we can say $-ni_L$. And here the i_L is nearly constant. So, we can write n I_o. Now, during that time, what happens is that Since this i_L current is now equal to negative of i_p current, so that is when my DR1 at $t = t_5$ will cease to conduct. And then it will stop conducting, it will go reverse bias. So, during this time, we can now write

$$t_{45} = t_5 - t_4 = \quad = L_{lkg}\frac{I_o}{v_L}$$

So, this is the time t_{45} we have with us. so we have time t_{45} we have time from t_{34} we have time from t_{23} , so we have all the times you know with us and we will we can do the analysis with this during this time it is minus mean applied and since both the diodes are on the V_R voltage applied across this inductor is actually zero still it is zero and at $t = t_5$ what happens is that the mode 6 will start at $t = t_5$ this this current is nothing but equal to the reflected i_L current from the secondary side because at this point we can say $i_p = -ni_L$. Since my current in the primary is actually reflected from i_L , so because of this thing DR1 gets reverse bias and then whatever the current is coming from here is actually we are having the current which goes from here comes over here comes back and then goes there the entire the i_L will be nothing but equal to i_{DR1} the entire current is flowing through the DR2 and since the entire current is flowing through DR2 the V_R voltage which is appearing will be nothing but here it was nvin so here also it was nvin voltage which will be appearing across this inductor.

And then we can do the volt second balance across the inductor and then calculate the how the output voltage varies with respect to the duty ratio D here if you look very carefully in this part

see V_R turning off the S1 switch here if we recall our you know i_L case exactly at t_2 my V_R voltage has to come up the V_R will be must reflect the V_{AB} voltage but since my i_p current is not equal to this i_L current the i_L current has to find the pathway that's when both DR1 and DR2 is conducting the V_R voltage or the rectified voltage after this DR1 and DR2 is 0.

So that's when this is the place from here to here this is the place where the duty is actually lost that means this particular thing has to come from here this rising has to come from here because the V_{AB} is coming from here but because of the because of the non-ideality that means because of the capacitance of these devices and because we wanted to achieve the ZVS (zero voltage switching) of these devices S1, we have to lose on something which is nothing but we are losing on the duty ratio.

Some duty is lost. That means whatever the output voltage we were assuming which was

$$V_0 = nV_{in}D$$

$$V_0 = nV_{in}(D - D_{loss})$$

where D_{loss} is corresponding to the time between D_{loss} corresponds to time. corresponds to time t_2 to t_5 which is nothing but summation of $t_{23} + t_{34} + t_{45}$. So, this is the disadvantage with this. Although we are achieving the soft switching of the leading leg, by default lagging lag, if we have sufficient i_p current and the L_{lkg} is sufficiently larger then we will also achieve the ZVS turn on of this lagging lag as well.

However the price which we have to pay is nothing but the actual duty which is getting lost and that's when our actual output voltage is slightly lesser as compared to what we could have achieved when we do not consider this short switching cases now let us see the how this thing will repeat itself after the time so in as of now we have discussed up till now we have discussed the diagonal switches S1 and S4 is actually changing its state now we will see when my S2 and S3 is actually changing my state so here what happens is that let us take after this point after this point the $V_R$is still be there the i_p keeps on going until this point and let's say and this S1 is still be there here S2 is still be there here and let's say at this point at this point let's say at this point

t_0 it was t_0 , so let's say at $t = t_6$ what you are doing is here it is still V_R. So, at $t = t_6$, what we are doing is here it is voltage $-V_{in}$ which is coming over here this is here at $t = t_6$ you have given the off pulse to the S1 switch since i have given the off pulse to S1 switch what happens is that this is t_6. Now the next timing instance let's say t_7 is when the capacitance C1 and C2 comes into picture in order to ensure the i_p is still maintained which is the negative that of the output inductor current.

So, because of that the inductor the i_p will still be there here and since my this V_{AB} will be falling down and this slope is

$$V_{AB} = \frac{I_1}{C_1 + C_2}$$

This slope it is falling and this is still be on at this point and because this is falling this will also falls down to this point. However, between t_5 to t_6 is very large. So this time period is very large.

So you can say this is something like this. Something like this very large value. Generally, the time distance between t_5 to t_6 is very large. Okay, and then after that, what happens is that since this voltage goes down to 0, the $V_{C1} = 0$, and the $V_{C1} = V_{in}$ voltage. That's when, because the current direction is reversed—here, the current direction is reversed. So the diode D1 will now be starting, and at that point, my diode D1 is starting.

So, after some point, we can start the S1 switch. This is nothing but my that time. Of the leading leg, and after this, my S1 is on now. The S3 is still on since the S3 is still on, and what you will see is that my $V_{AB} = 0$, during this period. During this period, the current is still going in this direction—let's say from here to, you know, from this point. Let's say this is at t_8; it is going, and $V_R = 0$ here at this point. Since my $V_{AB} = 0$. Now, at $t = t_8$, what happens? Since my $V_{AB} = 0$, this $V_R = 0$. Okay, so at $t = t_8$, what you do is you now turn off my S3. So from here to, let's say, t_8—from here to here, This you can say corresponds to δ value.

Okay, this is a phase shift. At that point, I am turning off my S3 switch. Since I am turning off my S3 switch, what happens is that in the lagging leg, the S3 switch—so because of that, the V_{AB}, the voltage across V_{AB}, will be nothing but minus of V_{C3}. And at that point, what you will see is that what you will see is that the L_{lkg} will now be resonating with the C3 and C4. As a result, what you will see is that this voltage—this one is minus VC3—so this $V_{AB} = V_{C3}$. So that's when the V_{AB} will be rising, and it reaches to V_{in} voltage. During that time, the current is actually having some slope, having some sinusoidal variation. Here also, it is rising with some sinusoidal variation; it is rising till this point.

And at that point, what happens is that the, you know, let's say after at this point, the V_{C3} voltage which is there is actually reaches to V_{in} voltage and V_{C4} voltage goes to 0. That is when you can turn on your S4 switch again to obtain the ZVS at that time lagging. Now at that point since my this is on so my S4 is on and already my S1 is on so you are now applying V_{in} voltage from there and that's when the current will rise equally and reaches to reaches to zero point which here t_9 we can say this is t_{10}. And after this zero this this one is nothing but slope is nothing but $\frac{V_{in}}{L_{lkg}}$ and after this thing it keeps on you know after this point after it reaches at this point at this place you are still you are this one is still on this one is still on it is still beyond this is beyond and it reaches at this point, reaches at this point where my i_p is nothing but reflected value of ni_L and as a result of it this will be keep on rising like this with a slope with a slope defined by

$$i_p = \frac{nV_{in} - V_0}{L}$$

with that slope it will be rising, and because of that slope what happens is that this voltage will keep on be zero at this point this point and this point and since at this point it is equal to this one, at this point myDR1 my DR2 which was also on will now get reverse bias and because of that my DR1 turns on and that's when here i am now having nV_{in} voltage applied across the DR and this will keep on after t_{11} it will keep on going and then after a certain point after Ts duration again you will this will come into picture however if you look very carefully from this t_0 to t_5 this

durations you know you can say this t_0 to t_5 durations are very t_0 to t_5 are smaller duration as compared to a small durations as compared to Ts this in order to you know to do it we have zoomed this particular waveforms so the same thing we got when we are doing the switching opposite devices switching i mean opposite which is you know S2 and S3 we are now going from S2 and S3 to S1 and S4 diagonal switches S1 and S4 So this is how the entire SFB operating modes are there. And if we try to find out the summary, we have in mode 0, we have S1 switch, S4 switch and DR1 is conducting in mode 1.

In mode 1 you have removed the pulse from S4 switch. So, you are now having C1 and C2 switch from the leading leg to coming into picture and then you have you know DR1 which will be still be in conduction in mode 2 So we can write it is D2. Again, here my S4 switch is still be there. S4 and DR1 is there. In mode 3.

In mode 3 what happens is that. My S4 switch is now turned off. Because of that I have D2. And in mode 2 only. We will now move from D2.

Since D2 is there. We can now give pulse to S2 switch. So we saw that. We moved from in the leading leg. We moved from S1 to S2 switch.

In mode 3 what happens is that we now remove the pulse from S4 switch because we are now have to turn on the S3 switch so we have now S2 switch and since the S4 pulses are removed we have C3 comma C4 capacitance coming into picture and since my C3 and C4 capacitance are coming into picture the $V_{AB} = - V_{C4}$ voltage and that's when my i_p current will no longer be equal to the reflected i_L current so that's when my DR1 and DR2 is in conduction then comes my mode 4 in mode 4 my C3 is completely discharged, so by D3 is conducting. And then it is you know D3 is conducting and your DR1 and DR2 is conducting since my D3 is conducting we can now here somewhere we can turn on my S3 switch my S3 switch as well so that's when we can achieve this DR1 and DR2 in mode 5 in mode 5 my S3 and S2 is there my transformer current is keep on you know falling down going up to zero so still my S2 S3 DR1 , DR2 is conducting and finally we have mode 6 where our S2 S3 and i_p current is actually equal to the reflected current of the output inductor current that's when my DR1 ceases to conduct and that's

when my DR2 is in conduction and that's when you go from S1 S4 DR1 to S2 S3 and DR2 switch So, this is the entire mode of operation of this PSFB.

In the other side, it is just the opposite of that and that is when we can able to understand the functionality of that. In this one, we have seen that in order to ensure my ZVS, we are providing some sufficient finite amount of time to the lagging leg, to the leading leg. Because of that, we are also having some duty ratio loss, which is we have also seen. some duty ratio loss which is from t_2 to t_5 duration t_2 to t_5 the duty loss the loss durations. Now if you look carefully in the leading leg we have defined the required condition to achieve the ZVS which is that time of leading leg has to be greater than t_{01}.

Which is you know. Which we can say greater than. $\frac{2C}{I_1}$.

That is a t that time of. Leading. And t that time of lagging. Is to be greater than t_{23}. Which is you know slightly bigger value which is

$$t_{23} = \frac{1}{\omega_1} sin^{-1} \frac{V_{in}}{I_2}$$

This is the term we have, and if we want to achieve this ZVS of lagging switch, we have to provide some finite value of that time in the lagging switch, which is greater than t_{23}. These are the required conditions here, and here are the required conditions. Now, let us see what is the necessary condition. So, the necessary condition

For ZVS of, let's say, first we will define the leading leg. Now, if we look very carefully in, let's say, mode 1, if you go to mode 1 and see In this case, what is happening is that my C1 and C2 capacitors are changing their state. That means C2 voltage is falling down from V_{in} voltage. C1 voltage is rising from 0 voltage, and that is using the i_p current, which is actually flowing through the series combination of L_{lkg} and L. So, we can write down that We can write down the energy which is there in the inductor is nothing but $L_{lkg} + \frac{L}{n^2}$ which is reflected onto the primary side.

$$I_1^{\,2} = L_{lkg} + \frac{L}{n^2}$$

And this is nothing but equal to I_1^2 because we were having the I_1 current during that time. And that has to be greater than half C1 V in square plus half C2 V in square.

$$\frac{1}{2}\left(L_{lkg} + \frac{L}{n^2}\right)I_1^2 > \frac{1}{2}V_{in}^2 C_1 + \frac{1}{2}V_{in}^2 C_2$$

That condition must satisfy because that energy has to be taken out from the C2 capacitance and has to be put into the C1 capacitor in order to ensure the diode D2 turns on. Once the diode D2 turns on, you have the voltage across S2 switch equal to 0, and that's when you can turn on the S2 switch. Similarly, if we look carefully, the necessary condition for ZVS of lagging leg, during that lagging leg time, if we see very carefully in the lagging leg time, in mode 3, we are talking about it is the L leakage which is coming in resonance with the C3 and C4. So, we can write down here in this case, the necessary condition is

$$\frac{1}{2}\left(L_{lkg}\right)I_p^2 > \frac{1}{2}V_{in}^2 C_3 + \frac{1}{2}V_{in}^2 C_4$$

that is the necessary condition for this particular scenario this much energy need to be sufficiently enough to ensure the C3 voltage discharges to zero and C4 voltage charges to be in that means in order to ensure this hundred percent ZVS of the lagging lag against ZVS during turn on i am only talking about during turn on because turn off automatically because of the capacitance C1, C2, C3, C4 our switches are going through the zero-voltage switching. So now if we can ensure that doing turn on this this condition happens then we can ensure that we are also having gvs of the lagging switch. So out of the leading and lagging lag the leading lag switches achieves ZVS turn on easily as L value is large enough and i_L current is reflected load current. However, for the lagging lag switches, since only L_{lkg} is coming into picture, the i_p has to be sufficiently large enough which becomes difficult during light load conditions. So, that is why we can write that it has the problem.

So, that is why this particular system of the lagging lag, again ZVS during turn on, I am only talking about during turn on because turn off automatically because of the capacitance C1, C2, C3, C4, our switches are going through. the zero-voltage switching or having the limited dvdt but during this time turn on it is a problem. So now if we can ensure that during turn on this this condition happens then we can ensure that we are also having ZVS of the lagging switch we

have light load condition that means my i_p is that I_2 value or i_p value is very small light load condition or you can say that small L_{lkg} or you can say large C3 and C4 or you can say high input voltage or large input voltage. So, during that time this lagging lag has problem. However, the leading lag does not have problem because it is this output inductor is coming in series with L_{lkg} and along with that the output inductor current which is reflecting is coming to actually taken out the energy from the C2 capacitor and putting the energy into the C1 capacitor.

So, this is the necessary condition for achieving the ZVS of leading and lagging lag. However, the required condition we know already the required condition for leading leg is $dead\ time > t_{01}$ time and for lagging leg the $dead\ time > t_{01}$, t_{23} times you know so that has to be ensured that required. So, after ensuring this necessary condition holds true that condition is required from the person who is actually designing that time now in all the things we have understood that in order to achieve this ZVS there is a duty loss from t_2 to t_5 period, so now let us quickly define the duty loss corresponding to that and that's when we can end our this lecture so we can we know that we can write our duty lost to be we can just say

$$duty\ loss = \frac{t_5 - t_2}{\frac{T_s}{2}} = \frac{t_{23} + t_{43} + t_{54}}{\frac{T_s}{2}}$$

And this value we can put in here. We can take one more approximation that t_{23} is smaller, small values as compared to t_{43} and t_{54}. Why? Because during t_{2-3}, we are doing the resonance between L_{lkg} and C1 and C2. L_{lkg} will be in generally it is tens of microhenry.

Most of the cases, not always, but most of the cases L leakage in case of high frequency transformer is in tens of microhenry. And our C1 and C2, I mean the output capacitances of the devices are nearly very small. So the frequency of resonance is very high. So that's when your t_{2-3} is very small period we can take. So our actual is nothing but t_{43} and t_{54}.

So this one we can write

$$t_{2-5} = t_{43} + t_{54}$$

$$= \frac{L_{lkg} i_p(t_3)}{V_{in}} + \frac{L_{lkg} i_p(t_5)}{V_{in}}$$

$$= \frac{L_{lkg}}{V_{in}}\left[I_2 + nI_2(t_5)\right]$$

$$I_1 \approx I_2 \approx nI_0 \; ; I_2\left(t_5\right) \approx nI_0$$

$$t_{2-5} = \frac{L_{lkg}}{V_{in}}\left[2nI_0\right]$$

$$D_{loss} = \frac{t_{2-5}}{\frac{T_s}{2}} = \frac{\frac{L_{lkg}}{V_{in}}\left[2nI_0\right]}{\frac{T_s}{2}}$$

$$D_{loss} = \frac{4L_{lkg} nI_0 f_{sw}}{V_{in}}$$

So this is what we got so what we understood from here in order to achieve ZVS to achieve ZVS L_{lkg} has to be more. Now, if my L_{lkg} is more, my D_{loss} value will be more. And if we look very carefully, so I will lose more D if I will go for, you know, good, very large value of L_{lkg} in order to ensure the lagging lag also goes to ZVS during turn on. Here we can also see if my V_{in} is increased. So, my D_{loss} is actually goes down we can also see that if my i not increases my D_{loss} increases that means for larger loads my D_{loss} will be more we can say here we will also see that if my you know if my switching frequency is more my D_{loss} will also be more we can say from this particular expression.

To achieve, if one wants to have Xevious of both the legs, they have to compromise on the loss. And we know that my V_O value is $V_O = nV_{in}(D - D_{loss})$. Because that amount of D_{loss}. So we have seen that what different modes of phase shift full bridge converter we have also understood what are the necessary conditions to achieve gvs turn on of leading and gvs turn on of lagging lag we have also seen what are the required condition that means what are the required value of dead time to be given to achieve the gvs turn on of leading lag switches and lagging lag switches

And then we have seen that in order to achieve those ZVS, we are losing some of the duty ratio. And we have then also come up with the expression for duty, the amount of duty which is

lost. And then finally, we have understood all the different modes of operation of PSFB. In the next class, in the next lectures, we will see the closed loop control and other aspects of PSFB. Thank you very much for patience listening to this lecture.