CHARGING INFRASTRUCTURE

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Week-08

Lecture-37

Lec 37: Phase Shifted Full Bridge (PSFB) Converter- I

Hello everyone, welcome to lecture number 37 of this NPTEL lecture series on charging infrastructure. In this lecture, we will study the phase-shifted full-bridge converter, which is one of the commonly used isolated DC-DC converters. So, we will see its operation and try to understand how and why it is being used. Now, if we recap our last few lectures, what we have studied, we have studied about the different PWM methods which can be applied to full-bridge converters. So, PWM strategies for full-bridge converters, we have seen that, and then we understood effectively there were nine possibilities there. Out of those nine possibilities, they can be grouped into two types of PWM called PWM type 1, which includes strategy numbers 1, 2, 3, and then we have PWM type 2, where we have 4, 5, up to 9 possibilities. Now, in this PWM type 1, we have seen that the diagonal switches, which are the diagonal switches in the full bridge, turn off at the same time. In type 2, the diagonal switches turn off at different times.

At the same time, different times, you can say, or staggered turning on. We can also say that at different times. Now, because of these two things, what happens is that we have understood that in case when we have type 1, we were having zero voltage switching during the turn-off case. However, we were not getting ZVS when it is turning on all four switches. That means the possibility of achieving soft switching is very minimal, or it is not possible, we can say, in the type 1 PWM where the diagonal switches turn off at the same time. However, In the type 2-based PWM, we have seen that at least the leading leg is surely achieving the ZVS turn-on, while the lagging leg may or may not, depending upon the energy associated with the leakage inductance and the transformer primary current. Depending upon that, the lagging leg also may or may not get ZVS turn-on.

However, in the turn-off case, all the switches will go through it because you have the output capacitance. Because of the output capacitance, it will achieve. But during the turn-on, only the leading leg will surely achieve zero voltage switching because The output inductor, which is enormously larger compared to the leakage inductor, is coming in series with the leakage inductor. And that's when it comes at the output of the leading leg half-bridges, and that's when we can easily ensure that the voltages change from V_{in} to 0 or 0 to V_{in} accordingly. And that's when we can ensure the body diode of the MOSFET turns on, and that's when we can, the moment the body diode turns on, we can ensure that the switch will turn on with zero voltage across it.

So, mostly in lighter load conditions, in some of the designs when the leakages are very small or when the output capacitance of the devices is enormously higher and if the input voltage is very large, then during those cases, the lagging layer will find difficulty in achieving zero voltage switching during turnoff. So, you know, if you want to achieve soft switching, the possibility is very high, much higher in the case of PWM type 2 compared to PWM type 1. Now, another way of controlling the full bridge converter is by doing phase shift modulation. Now, in the phase-shifted base modulation, what happens is that we are not changing the duty ratio of the switches S1, S2, S3, S4. In the previous case, if you recall, we were actually changing the turn-on period of those switches and accordingly we would get the required voltage at the output. But in this case, what we are doing is keeping the turn-on fixed at—we can say the turn-on of S1, S2, S3, S4 is fixed at $\frac{T_S}{2}$ period and turn-off is fixed at $\frac{T_S}{2}$ period. However, we are providing the phase shift between, you know, we can say again, we can use the same nomenclature: leading leg and lagging leg.

We can provide the phase shift between the leading leg and the lagging leg and control the output voltage depending upon the amount of phase shift we are giving between the leading leg and the lagging leg. So, what I mean by that is, let us see. So in this, here we are assuming ideal switches. And then we will start introducing the non-idealities, like, you know, output capacitances and leakage inductance of the transformer, and see their effect as we go along. But as of now, we will consider that these switches S1, S2, S3, S4 are actually ideal switches.

That's when, when S1 turns off, we turn on the S2 switch, and since we are turning on the S2 switch, this turns on for a $\frac{T_S}{2}$ period. This entire S2 switch turns on for $\frac{T_S}{2}$ period. During that time, if you look very carefully, when S1 turns off and S2 turns on, the switches S3 and S4 are not changing their state. The switches in the lagging leg, which are S3 and S4, will change their state, meaning S3.

So, S3 will actually be, you know, turning on at point t equal to t2. Now, since my S3 is turning on at $t = t_2$, what happens is that from t_0 to t_2 , what is happening? My S2 and S4 switches are on. So, we can also say that if we look very carefully in the leading leg and lagging leg, we are actually doing the phase shift of, you know, indirectly. We can say we are actually turning off the diagonal switches with a certain phase shift. Let's say by phase shift by angle δ.

Now, this δ, what is there? We can write it to be

$$\delta = \frac{t_2 - t_0}{\frac{T_s}{2}} = 180^0$$

and it has been there for 180^0, because in $\frac{T_s}{2}$ period, we are actually encompassing 180^0, and in the entire $T_s$period, we are actually encompassing 360^0. So, the portion of $\frac{T_s}{2}$, that means t_0 to t_2, that is the angle δ, you are giving the phase shift between turning off of the diagonal switches in, you know, in the full bridge converter. So, this is the turning off of S1 and S4, which is actually shifted from each other by an angle δ. Before that, when S1 and S4 were on, we were actually applying, you know, from V_{AB} voltage, we were actually applying when S1 and S4 were on. These two are on, then you are actually applying V_{in} voltage from V_{AB}.

And since V_{AB} is applied over here, this DR1 gets forward bias, and that's when, you know, at this place, at this place, we can get, you know, nV_{in} voltage, where $n = \frac{N_s}{N_p}$. So, nV_{in} voltage is applied at one end of the inductor and another end via V_o. So, here we can say that my voltage across L is

$$v_L = nV_{in} - V_o$$

And the inductor current will then rise, you know, linearly with the positive slope. So, we can say the inductor current will rise linearly, something like this, by $\frac{nV_{in}-V_o}{L}$ then what happens in between t_0 to t_2 between this t_0 to $t_2$what happens is that we have actually turned off our S1 and we have turned on our S2 switch and our S4 is still on we are not turn off S4 switch the moment we are turning off S1 switch we are pushed the turning off of S4 switch by certain angle δ. Now during that time what happens is that the S2 and S4 is on. So during that time the S2 and S4 is on. During this time since my S2 and S4 is on we are actually applying across V_{AB} in this loop.

If we do KVL we apply it is nothing but 0 voltage which we will be applying from the V_{AB} . Since we are applying a zero voltage from V_{AB} , the inductor current has to find the, you know, this path to flow. That's when they got distributed among DR1 and DR2. And as a result of this, the V_R $(V_R = 0)$ voltage is nothing but zero. At that point, myv_L, is $v_L = V_O$.

And you will see that during this time, my inductor current is actually falling to this place. So here it is $\frac{nV_{in}-V_o}{L}$ and here it is $\frac{-V_o}{L}$. It is falling. And then again at $t = t_2$, I have turned off my S4 switch. Since I have turned off my S4 switch, I will now turn on my S3 switch. So the S3 switch is on and since S3 switch is on, so S3 is on and S2 is on.

And because of that, you are now applying minus V_{in} across AB . And because it is $-V_{in}$, what happens is that DR1 gets reverse biased and DR2 gets forward biased. And as a result, what happens is that across V_R, we are again applying nV_{in} voltage across it. And then after that, again in the next cycle, we are now applying zero voltage from V_R.That's when here again, my v_L is,

$$v_L = nV_{in} - V_o$$

and here it is my $v_L = -V_o$

So, from this particular expression, what we can write is my δ value is $\delta = \frac{t_2 - t_0}{\frac{T_s}{2}} = 1 - D$

we can take it there, and this value, when you look from this particular relationship, it is

$$\frac{\delta}{180^0} \cdot \frac{T_s}{2} = (1 - D)\frac{T_s}{2}$$

So, which indicates that the phase shift is kind of directly related to the duty ratio D. So, we can say that if we increase this delta, then what happens? For more amount of time, my $V_{AB} = 0$. That means my $V_R = 0$.

That means we can say that my $(1 - \frac{D)T_s}{2}$ period is more. That is when if we do the calculation, $V_O = nV_{in} * D$. So, D will be smaller, and that's when we can say that the output voltage, which is V_O, is less. So, if we increase this δ, the phase shift, we will reduce the output voltage, and that is when we can do one more kind of modulation. If you look carefully, the turn-on time of S1, S2, S3, and S4 switches are kept the same as $\frac{T_s}{2}$.

S2 turns on time is $\frac{T_s}{2}$. S4 turn on time is also $\frac{T_s}{2}$.. So, we are not changing the turn on period. It is kept at $\frac{T_s}{2}$.. but it's the time during which it is turned off they are actually shifted by the angle δ and which is actually leading to the output voltage variation so this is one way by which you can get but here if you look very carefully since i am turning off my diagonal switches at different times actually we are having the PWM type 2 kind of thing we have and this we use to achieve you know zero voltage switching of devices if you look here very carefully it is you can say PWM type 2 type 2 scheme and it is nothing but type 3C or you can say modulation strategies 9 strategy 9 what we are talking about here in case of phase shifted full brief if you look very carefully this is very easy to implement, because you do not have to change the turn on time of your switches you can keep a turn on time of the switches to be $\frac{T_s}{2}$. However, you are just shifting the turn off time of the diagonal switches similarly for S2 and S3 you will also be shifting the turn off time. So, this modulation scheme called as a phase shifted modulation, so here what we have we are actually keeping our turn on time of the all the force switches to be

$\frac{T_s}{2}$ and only giving the required phase shift between the turn off time of diagonal switches that means S1 and S4 or S2 and S3. So, that phase shift has to be given equally between S2 and S turning off between S2 and S3 and turning off of S1 and S4. Now let us try to you know see how this particular converter works at in different modes.

Let us try to discuss in detail. So in this one the first mode is obviously we were assuming that S1 and S4 is conducting So before $t = t_0$ what we are doing is we are your S1 and S4 was on the let's say these are MOSFETs , so channel is already formed and the current is actually flowing through the channel and this is the i_p current through the L_{lkg} and this is the i_L current, So we can say that my i_p is actually the i_L current reflected onto the primary side and it has the rising slope and now what happens is that since these two switches are on the V_{AB} is nothing but equal to V_{in} voltage we have and this V_R is nothing V_R is again this point we are this voltage this V_R is nothing but nV_{in} which has been applied.

Now at $t = t_0$ the S1 is turned off that means the gate pulse to S1 is removed so what happens is that this is the current which is there is which is coming like this i_p current it is actually going and it is going through this channel here on this side and what we see is that on this side because the current is coming out of this half bridge the in the capacitance C1 and let's say this is C2 this is D1 let's say this is D2

So in C1 C2 the current will be going in this direction and C2 it will be in this direction. Now because of that what we will see is that if we recall in the previous case our in this case my V_{C4} is actually at in this case $V_{C4} = 0$, $V_{C4} = V_{in}$, and we can say V_{C1}you know all the capacitor C1, C2, C3, C4, $V_{C1} = 0$ and $V_{C2} = V_{in}$ because you know this is on means the entire voltage will coming across this capacitor C2. So, in this case what happens is that here the C2 is actually discharging from voltage Vin and we can say that the V_{C2}voltage is decreasing and because the current is in this direction the C1 is charging from you know zero voltage and we can say V_{C1} is actually increasing now because of that what happens is that since in this case

if we look very carefully this V_{AB}. V_{AB} is nothing but equal to, you know, if you take the loop in this direction, $V_{AB} = V_{C2}$. And since the V_{C2} is discharging from $V_{in} = 0$ voltage, what we are seeing is that V_{AB} is also falling down. And this falling down, if we take the slope, you know, $\frac{dv}{dt}$ of this particular thing, this $\frac{dv}{dt}$ is nothing but equal to This current i_p which was there at we can say t_0. Let us take this i_p current is let us say i_L.

So, we can say this i_L by because of this capacitance both the capacitance we have C1 plus C2. So, we can say this slope is nothing but i_L by C1 plus C2. With that slope this voltage is falling. And since my V_{AB} is falling and again during that time my S4 is on. So, S4 is on only.

So, because of that, since i_p is actually going in this direction, which is again the reflected current from the output inductor. So, what we can say is that this i_p will remain nearly constant because we assume that L is large, and that is when we can say the i_L ripple is very small. The ripple current in the inductor is very small. So, hence we can say the i_p is nearly constant, and let us define this number to be i_L, and this is nearly constant. This slope is actually limited by this current i_L, which is coming out of the bridge and the C1 and C2.

And so, what we saw the moment we give turn off of this S1 switch, turn off of this S1 switch, we can say that this voltage at the output of this bridge, which is V_A (let us say V_{AN}), is actually having the limited $\frac{dv}{dt}$ at the output of the bridge. Then, if you look very carefully in this particular system, if you try to see what is the scenario which is happening, we can write it down in this way. This is i_p, C1, C2, C3, C4, D1, D2, D4, and D3. And since we have not discussed about V_R, since my diode DR1 is on, this V_R, voltage is actually the reflection of what is there in the V_{AB}, which is also falling to zero, so we can write it down. $i_p(t_0) \approx i_p(t_1) \approx I_1$. And we know that the V_{C2} is actually discharging, and V_{C1} is actually charging, so we can write down this

V_{C1} (I mean, obviously a function of t) that is charging from zero voltage, and it is charging with the current i_L. We can write

$$V_{C1}(t) = \frac{I_1}{C_1+C_2}(t - t_0)$$

Both the capacitors C1 and C2, and in this particular period, we can say that it is nothing but $(t - t_0)$ because it is rising linearly because this current is constant, so it will rise linearly. So, now we can say that this equation we can say, and in this particular equation, if we assume $C_1 \approx C_2 \approx C$, we can say that

$$V_{C1}(t) = \frac{I_1}{2C}(t - t_0)$$

And the rate with which it is charging, V_{C1} is charging in the same manner as V_{C2} is discharging. So, we can say that V_{C2} is nothing but my Vin voltage minus my V_{C1} voltage. So, because if you do the KVL in this loop, the $V_{C2}(t)$ is

$$V_{C2}(t) = V_{in} - \frac{I_1}{2C}(t - t_0)$$

And we can say that at $t = t_1$ at that point, at this point, what happens is that the entire, you know, $V_{C1}(t_1)$ is actually is, you know, charged to V_{in} and we can say $V_{C2}(t_1)$ is actually becomes 0.

$$V_{C1}(t_1) = V_{in}$$

$$V_{C2}(t_1) = 0$$

So, this is the end of this period what we see that because of the constant current coming out of this bridge why the constant current because the output inductor current is actually getting reflected. That means in other words you can say this L_{lkg} and this output inductor L is coming in series. And that both these inductor along with this the load current which is enormously higher we will get good amount of energy which is been there with them and which is actually charging the C1 capacitor and completely discharging the C2 capacitor to 0.

That is when my D2 gets turned on and that is when we can get S2 to be turned on with the 0 voltage switching. So at $t = t_1$ we will get this particular scenario which is shown over here

and we can say that the time between in this equation if we write, so we can say the time between t_0, t_1 we can just write because this is nothing but $t = t_1 - t_0$ is

$$\text{At } t = t_1 - t_0 = \frac{2CV_{in}}{I_1}$$

This time, we must provide this time because in this time, the C2 voltage is actually going to 0. After t_{01}, the V_{C2}=0. That is when the diode can turn on. And if the diode turns on, we know that the S2 will go for zero voltage turn on because the diode because since the diode turns on the voltage across S2 is actually zero so now what happens is that.

Now let us take the next mode where what we are doing is since the voltage ofV_{C2} goes to 0 the diode D2 which is here D2 C2 C1 D1 C3 D3 C4 D4 so here since the V_{C2} goes to 0 the diode D2 turns on and that t_2 turns on to meet the i_p current. So here in the previous case we can also say that in the previous case we can in this case we can also say that $i_P = i_{C1} + i_{C2}$,which is coming out of this half bridge however in this case i_{C1}will no longer be conducting and this voltage is nothing but V_{in} so we can say that V_{C1} is actually v in at this point at $t = t_1$, so we can say that during that time the diode D2 turns on and you can say the i_{D2} is completely equal to ip current which is coming out of the half bridge So, this is what we will see in this particular case where what we see is that this diode gets turned on. However, the S4 is still on. Since diode turns on, since D2 is on, after some time, now what is the time?

We will see that after some time, the switch S2 can turn on. Turn on with zero voltage switching why i am saying zero voltage switching because the moment diode turns on the voltage across this drain to source of this switch is actually equal to zero because the this diode is already on since the diode is on the voltage is nearly zero or i mean some forward voltage of diodes are there but you can imagine it to be very small maybe two to three volt as compared to v which is some 400 or 500V more than 400V So that is nearly 0. So what we are seeing is that the diode turns on.

So after some time we can give the switch as to gate pulse. So, in the previous case if we see in the first case if we see the first case mode 0, S1 was on. we have removed the gate pulse from

the S1 such that in order to maintain the i_p current C1 and C2 comes into picture and during that time there were no gate pulses to be given both to S1 and S2 and they will be only given after certain you know once the diode turns on the point after which the S2 gate pulse is given is nothing but that time. So, what happens you can give this gate pulse before itself before this also. However, if you give before t_1, then what will happen is that the voltage across this C2 will not be equal to 0. That is when the diode will not get turned on and whenever you turn on the S2 switch, you will see certain finite switching loss across this device S2.

So, we can say that because this is there, if we can ensure in that time, If the given dead time, that means the time after which the gate pulse of S2 switch can be given logic 1, the dead time is greater than t_{01} which you can say that that time is greater than you know t_{01} if we try to recall what is $t_{01} = \frac{2CV_{in}}{I_1}$,

if we can ensure these two conditions is there then the ZVS term on off S2 switch is possible,

$$\text{so, } dead\ time > \frac{2CV_{in}}{I_1}$$

is the required condition that one must provide in order to ensure that this C2 voltage V_{C2} voltage the voltage of the capacitance C2 goes to zero that's when diode turns on and when the diode turns on you can have the zero voltage across the switch and then you can give the turn on pulse to the S2 switch. So we can say that after some i mean after some time or just right after the t_1 duration at that point also you can give any pulse or at at $t = t_1$ which is the boundary condition of that time at that point also one can give where you will receive you know nearly zero voltage switching however if we ensure that that dead time is greater than this one this hundred percent ensures that we are achieving the zero voltage turn on of the switch S2.

Now, you have given the gate pulse. So, once you give the gate pulse, this device gets turned on. This diode D2 will move from this conduction path of this current i_p. So, we can say that, so after some time, between t_1 and t_2, the gate pulse to S2 can be given which ensures ZVS turn

on off S2 switch or you can say in other words leading leg switch because the same thing will repeat in the other way around when we are going from S2 to S1

So, we can say that in order to achieve the ZVS, to ensure ZVS, we must ensure that the

$$dead\ time > \frac{2CV_{in}}{I_1}$$

where C is nothing but C1 equal to C to the output capacitance of the devices, if we assume the same devices we are using. and this is the dead time for the leading leg only for the leading leg we are not talking about switches of the lagging leg lagging leg switches is still on S4 is still on this lagging leg. So, it is a dead time for the leading leg has to be

$$dead\ time > \frac{2CV_{in}}{I_1}$$

which ensures that my this particular thing is happening and we can if we take the i_L current to be nearly equal to I_0 current so we can say that the I_1 is nearly equal to I_1 reflected onto the you know this i_L which is reflected onto the i_P so you can say that i_P is nearly equal to N times i_L So, since my i_L is nearly equal to I_0, we can say that I_1 is nearly equal to $n\ I_0$. So, from there we can calculate this $n\ I_0$ and from there we know that what is my dead time for the leading leg.

Now, since my S2 switch is turned on, so what happens is that it goes on up to this T2 point and at T2, at T2, at T2, at T equal to T2, the switch S4, that means.

Now we are dealing with the lagging lag switch S4, which is a lagging lag switch. switch the gate pulse of that turns off the gate pulse of S4 switch gets removed and since here I have already given the gate pulse of S2. So, you can see on the leading leg my S2 is already on and now after certain point after at $t = t_2$, that means between t_2 to t_0 is nothing by my δ you know phase shift because is nothing but equal to the phase shift we are giving from t_2 to t_0. However we see that what will happen is that since we are turning off my S4 switch again this the output capacitance of S3 switch and S4 switch C3 and C4 will now start appearing across it now if you look very carefully till this point my i_L is there however in this case what happens is that since my C3 and C4 capacitance is coming here and we have the i_L current which is going

like this on this side now this ip current will come here and it will come on this side and goes to C4 in this direction and goes to C3 in this direction i mean from here it goes to the top direction and if you recall previously case here this was off . So, V_{C3} we can say in this case $V_{C3} = V_{in}$ and $V_{C4} = 0$.

Now here what happens is that C3 is discharging from vin voltage and C4 is charging from zero voltage because of the direction of the current. Now Since and we can say that here in this case my V_{AB} voltage since my S2 is on the $V_{AB} = - V_{C4}$ voltage VC4. And since I am now applying minus V_{C4} voltage which is coming in and which is actually since my V_{C4}voltage is charging my V_{C4} voltage is charging that's when you will see that my V_{AB} is actually going in this direction. And since it is going in this direction, this $V_{AB}$is actually going in the negative direction, the i_P will no longer be equal to, you can say that here $V_{C4}$is increasing. Since my V_{AB} voltage is negative applied across the leakage inductance, across this V_{AB}, so we can say that i_P will no longer be reflected i_L current, or output inductor current, which is here. Now, since i_P is not at all equal to i_L, so in order to ensure this current to be continuously flowing, this i_{DR1} and i_{DR2} both gets turned on and we can say that $i_L = i_{DR1} + i_{DR2}$. Both, we can say that this indicate DR1 and DR2 gets forward bias and since they got forward bias, the V_R ($V_R = 0$) voltage which is over here is actually is nothing but equal to 0, and if you see in the previous section the V_R voltage here V_R voltage if you see the this one the V_R voltage which is over here is nothing but the reflected voltage from the V_{AB} which is coming from here which is actually zero here if you see in the previous in you know in this mode also in mode one also it is nothing but this $V_R$voltage is the same thing which is following by V_{AB} and previously also it is the reflected voltage what we have seen from the V_{AB} which was nV_{in}.

So, in the mode 3 is despite the vab is increasing in the reverse direction the V_R is still $V_R = 0$, because in order to ensure the inductor current to be flowing both DR1 and DR2 gets forward by that's when my V_R is still be equal to 0. Since this voltage V_R voltage is 0. Similarly since

both the diodes are on this entire secondary side winding get short circuited like this since because of this short circuited what happens is that the voltage across this is nearly zero and we can say that the entire V_{AB} is imposed upon is imposed upon a leakage the entire V_{AB} is imposed imposed upon a leakage and we can also say that in this way this L_{lkg} is actually in this circuit it is going in this direction coming like this and some portion is is actually since some portion goes over here and some portion goes over here this comes from here and from from here it comes back some portion goes from here it actually comes to here. So this is what we get in both the things what is happening is the L_{lkg} is in resonance with C3 plus C4. And if you look in this one, since L_{lkg} is in resonance with C3 and C4, so this current, i_p current which is going in this direction coming out of this point B, some portion is going through C4 and comes back from the S2 switch to the, back to the loop.

While the other portion of the current is going through the C3 via the source V_{in} and through the S2, it comes back to the inductor L. So, if you see in this loop, it goes here in this way. comes back while the other portion comes from here goes here in this way and then comes to V_{in} and goes over here this way. So, if we write if we try to see the equivalent circuit it will look like we have a L_{lkg} And then we have a C3 capacitor and C4 capacitor is coming parallel to C3 because the portion of the current which is coming at this point is going, some portion is going to C3 and C4. And that is when is actually getting connected in this manner.

And this particular thing, we can say that that is nothing but your $i_p(t)$. So, this is the way by which, you know, you can define your equivalent circuit. And then we can write this. If you look very carefully in this thing, if you define this as I_2 and this I_2 is actually the peak value of the current from here. So, we can just write

$$i_p(t) = I_2 cos(\omega_1(t - t_1)).$$

where we can say ω_1 to be

$$\omega_1 = \frac{1}{\sqrt{L_{lkg}(C_3+C_4)}}$$

So, we can just write the resonance frequency is nothing but L_{lkg} , C3 plus C4 and it is only happening because my L_{lkg} is now is coming in resonance with this thing. So since this ω_1 is you can say that a resonance frequency. And so here we can say $C_3 \approx C_4 \approx C$ and that's when we can write my omega 1 to be.

$$\omega_1 = \frac{1}{\sqrt{2L_{lkg}C}}$$

And then if you look very carefully this i_p we got so we can just write $v_{C4}(t)$ to be since this i_p current is charging two capacitances we can write 2C both C3 and C4 integration my i_p current which is

$$v_{C4}(t) = \frac{1}{2C}\int i_p(t)dt$$

$$v_{C4}(t) = \frac{1}{2C} I_2 sin(\omega_1(t - t_2))$$

$$v_{C4}(t) = \sqrt{\frac{L_{lkg}}{2C}} I_2 sin(\omega_1(t - t_2))$$

And then we can calculate $v_{C3}(t)$.

$$v_{C3}(t) = V_{in} - v_{C4}(t)$$

$$v_{C3}(t) = V_{in} - \sqrt{\frac{L_{lkg}}{2C}} I_2 sin(\omega_1(t - t_2))$$

So, with this voltage, $v_{C3}(t)$ voltage is going down, you know, this sinusoidal fashion it is going down and $v_{C4}(t)$, the voltage across the capital C4 is actually charging off with that sinusoidal manner. Sorry, I have done one mistake.

So, we will discuss the conditions for the dead time for this lagging switch because leading we have already defined the dead time condition. We will define these conditions in the next lecture. So, we will see you in the next lecture and thank you very much for patience in listening to this lecture.

Thank you.