CHARGING INFRASTRUCTURE

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Week-08

Lecture-36

Lec 36: Modulation Strategies for PWM Full Bridge Converter-II

Hello everyone welcome to the lecture number 36 of this NPTEL lecture series on charging projector and today we will continue our discussion on different modulation strategies for PWM full bridge converters so the last class we have seen different possibilities of pulse width modulation which is possible in the full bridge converters so for that we have defined two legs one is leading leg and another one is a lagging leg where leading leg comprises of switch S1 and S2 lagging leg comprises of switch S3 and S4 and we were getting the different modulation methods by actually adjusting the turn on periods of switches in the leading leg in the forward direction and that goes up to maximum up to ts by two however what we saw when we are doing the turn on time adjustment we see that there is no difference in the vab voltage that's when our v naught was kept at the same value which is n being times d similarly that i mean for the lagging lag we can adjust the turn on time of S3 and S4 switches in the backward direction that means falling edge we are delaying the falling edge in leading leg case we were actually moving the rising edge in the forward direction this we can say forward direction and in the lagging layer we can say that backward direction

By doing that, we can get different possibilities of modulation schemes. We could get from 1 to 9 modulation schemes and in that we have seen that in modulation scheme 1 to 3, we have seen that the diagonal switches which is S1 and S4 and S2 and S3 are actually turned off at the same time. However, in the modulation method going from 4 to 9, the diagonal switches are turned off at a different time. Now depending upon that there are two kinds of pwm type 1 and type 2, now let us take one by one how these PWM types look like ,now in this pwm type 1 and type 2 if we see very carefully as of now we haven't taken the consideration of this device

capacitances and the you know effect due to this leakage which it creates and this device capacitance which are you know C1 ,C2, C3, C4 which are there in the device because of its construction is automatically comes into picture.

Now, because of this capacitance the transition what we discussed in the previous lectures will not be the same there will be some difference because of this capacitance. So, because of that we will see that how this particular capacitance and this parasitic I mean this leakage inductances and this parasitic capacitance of devices impacts the switching of this lagging lag and leading lag. So you know we can say that in this particular type 1 case the diagonal switches diagonal switches which are you know you can say S1 S4 and S2 comma S3 switch are turned off are turned off at the same time. So, let us see how this capacitances will determine you know different operations like whether we will get the soft switching or not let us try to understand that and again here we have A and B point as we have discussed. Now, in the first case we assume that let us say we will define our let us say we will draw our you know

V_{AB} voltage whatever the voltage we are getting at V_{AB} and we will define our let's say the current which is going through the through the transformer primary is let's say i_p which is the transformer primary current this we will define as the i_p now if you look very carefully we will define a time $T_{0.}$ Now during the T_0instance what we can see is that the S1 and S4 is on so this is our leading leg and this is our lagging length so what we will see is that since the S1 and S4 is in operation and so whatever is here this I_L current which is there at the output that will be reflected in terms of $i_p$current and if we assume that this inductance inductance L is very big inductance L is large thus i_L is nearly constant And since it is nearly constant, we can say that i_p is also nearly constant. Because whatever the current which is there here will be actually reflecting on the i_p. So, whatever we have, we have V. So, the voltage across, you know, the voltage applied at the primaries at the point A and B is nothing but V_{in}.

This V_{in}voltage which is because this is on and this is on. So, this positive terminal is applied to A point and negative terminal is applied to the B point. So, we will have the V_{in} voltage which is

coming over here. And then after that what is happening is after this. So, we can also assume that i_p is nearly constant and which is the reflected current coming from the i_L.

So, i_p is also constant. And here S1 and S2 switches are in conduction. Since we are giving the turn off, since we are turning off both the diagonal switches and they are turning off at the same instance, so let us take how the system will look like. Since it is a type 1 PWM, we are turning off the S1 and S4 switches at t equal to 0. T_O so S1 and S4 are actually turned off now because the S1 and S4 turned off so if we say this is C1 this is C2 this is C3 this is C4 and current is actually in this direction i_p current as a result of which what happens is that in this bridge since in order to maintain the current the current will be drawn in this capacitor C1 in this direction and in the capacitor C2 in this direction

So, what it indicates, if we take the previous condition, in the previous condition, since my S2 switch was off, my V_{C2} is actually the V_{in} voltage and you can say my V_{C2} is actually equal to V_{in} voltage because since the S4 switch and S1 switch is on, so the V_{C3} and V_{C2} is V_{in} voltage. So, here what happens is that since my V_{C2} is at the V_{in}voltage at that time, so V_{C2} discharges. Or you can say the C2 capacitance discharges. C2 discharges that indicate V_{C2} is falling down. Falling down from V_{in}.

And C1 charges because of the direction of the current charges. So, what you can say the V_{C1} is increasing from 0 voltage. So, as a result of which this C1 and C2 is doing like this. Similarly, if you take on the other side V_{C3} , if it looks very careful in the previous case, V_{C3} was V_{in} and V_{C4} is actually 0. So, we will see in this also, the current will be in this direction going into the half bridge.

Since it is going into the half bridge, it is actually going here in this direction. And in this direction, it is going in, you know, in this direction, that means in this direction. What it indicates that, you know, the C3 capacitance, so C3 discharges, that means my V_{C3} is actually reducing

down from V_{in} and C4 charges. that indicates my V_{C4} voltage is increasing from 0 volt. Now at that time the V_{AB} voltage can be achieved by applying KVL in this loop comprises of the C2

L_{lkg} primary winding and this C4 which gives the you know the value which is somewhere around you know this subtraction of this V_{C2} and V_{C4} voltage and since the current i_p gets reflected from the output inductor it is nearly constant so we can say it is nearly constant and that is when you can see that the V_{AB} will be falling down with a slope defined by the charging and discharging of these output capacitances. So, we can see that the slope, you can see the V_{AB} falls with a slope nothing but

$$\frac{dv}{dt} = \frac{-i_p}{C_1+C_2}\frac{-i_p}{C_3+C_4}$$

that is a slope which which it will be falling down.

Now after this what happens is that this voltage when it goes completely to $-V_{in}$ at this point it goes to continuously going and become equal to $-V_{in}$. Now at t equal to t1 what happens is that during this time my $V_{C2} = 0$, $V_{C3} = 0$ as a result of which the current will now the i_P current the transformer current will now start flowing through the diode D2 and D3 and we can write D2 and D3 is in conduction. Now since the D2 and D3 is conducting this diode and this diode is conducting the V_{AB} voltage is actually nothing but minus V_{in} voltage which is been applied because the A terminal is connected to negative of DC link and B terminal is connected to the positive terminal of the DC link. So, that is when we will have the $-V_{in}$ voltage let us say up to certain point let us say define this as D2 point. And this because of this thing the current will now the i_p current will now actually be started to falling down. and it keeps on falling down and becomes equal to zero because of the fact that we are now applying a $-V_{in}$ voltage from here and since i_p is falling it goes below the value of reflected i_L current and becomes not equal to i_L current which is being reflected as in the previous case because of that what happens is

that this i_L has to find a path because this L is very large So because of that what happens is that the current after coming here gets divided into the top winding and bottom winding.

They both get distributed. So, we can say that $i_{DR1} + i_{DR2} = i_L$. So, both currents get divided into both the winding and since both the current divided into both the winding both the DR1 and DR2 is forward biased the entire secondary side winding is short circuited because of this there is no voltage I mean the voltage of the primary winding is actually zero. Now, since the voltage across the primary winding is 0, however at the terminal we are applying the $-V_{in}$ at the V_{AB} terminal we are applying $-V_{in}$. Since we are applying $-V_{in}$, this entire $-V_{in}$ is appearing across the leakage inductance spring across the leakage because at this side since the secondary side is completely short circuited the voltage at this point is actually the reflected voltage is actually zero. However from this side we are applying $-V_{in}$ and the current keeps on going and becomes to zero since the transformer current goes to zero the D2 and D3 diode will no longer be in conduction if the diodes are no longer in conduction we can write the D2 and D3 ceases to be in conduction. And we can write D4. And that is when capacitance C1, C2, C3, C4 will come into picture. And at the same time, the I-L current has to find the pathway.

As a result of which, the DR1 and DR2 will get forward bias and as a result of which, the secondary winding gets short-circuited. And as the secondary winding gets short-circuited, the voltage at this point, that means at the primary winding, you can say this to be V_P. We can also write this $V_P = 0$. And since $V_P = 0$, the entire V_{AB} is actually appearing across this L_{lkg}. And thus, in this circuit, C1, C2, C3, C4 will start resonating with L_{lkg}.

As C1, C2 and C3, C4 comes in parallel, so in this circuit, if you see, you know, the current is coming over here. It is coming over here. It goes here. So, C1, it comes back. and goes to a leakage.

Similarly, some portion of the current will also come from here, goes to here, then goes over here. Now, this is again it is in operation as C2 and C1 is in operation. So, as a result of which what you will see is that the L_{lkg} comes in resonant with C1, C2, C3 and C4 capacitance. And

because of this resonance, you will start seeing some sinusoidal variation in V_{AB} and some sinusoidal variation in $i_P$current.

So, let us draw that how the V_{AB} and i_P will look like. So, in this after reaching to this point and this point the current is zero and at that point it is L_{lkg} resonating with C1, C2, C3, C4 as a result of which in the current we will have something like you know some oscillations will be there and in this one also you know we have going like this. some oscillation. This is this we are drawing with decaying ratio because there is also some resistance in the winding of the transformer. So, we have the damping effect and that is when these oscillations die down.

This may die down, this may not die down. That is not in our control because $L_{lkg}$is actually resonating with C1, C2, C3, C4. There is no V_{in} voltage coming over here. There is no this side transformer winding is coming over there. Only this $L_{lkg}$and these four capacitances are there.

If we take the same sinusoidal behavior of V_{AB} and i_P, it will look something like this. This is showing our oscillations. So, we can say that it actually goes and reaches till this point. And then what happens?

Assume at $T = T3$. At T3, the switch S2 and S3 turn on. I mean, you have given the pulse to turn on S2 and S3. So, what happens in the initial case? We have suddenly turned off where S1 and S4 were in conduction. Then you remove the gate pulses from S1 and S4 simultaneously or at the same time. Because of that, all the capacitances are coming into conduction and the V_{AB} is actually falling with a limited slope. After that, the voltage of V_{AB} goes to negative because the diodes D2 and D3 conduct.

Since diodes D2 and D3 conduct because the voltage across $V_{C3} = 0$ and $V_{C2} = 0$, they are conducting. As a result, this i_P current is falling and it falls until it reaches the point zero. And at point zero, what happens is that this L_{lkg} comes into resonance with C1, C2, C3, C4. And as a result, you will see oscillatory behavior of inductor current, which is nothing but i_P. We have the oscillatory behavior, and similarly, the voltages across C1, C2, C3, C4 are also having

oscillations. As a result, at the V_{AB} , we will see some kind of oscillations, and these oscillations die down because of the resistance of this winding. Now, the V_{AB} voltage is oscillating, and these voltages will be appearing across S2 and S3.

And when at $T = T3$, S2 and S3 are turned on by giving gate pulses to S2 and S3, they may turn on with non-zero voltages across them. So, S2 and S3 may go to hard turn-on. That means they may turn on with some finite voltage. The S2 and S3 turn on with a non-zero voltage across them. So, since I turned on with non-zero voltage and since at this point we are turning on my S2 and S3 here.

S2 and S3 are turned on. That means we have given a gate pulse. So, at that point since S2 and S3 turn on, what happens is that this voltage goes to $-V_{in}$. And it remains there, which is $-V_{in}$, and the current because of that the current will actually go down and reach the minus, you know, whatever the reflection from the secondary side. So, what we understood with this kind of type 1 PWM is that the S1 and S4 when turned off, they turn off with zero voltage switching, but the S2 and S3 turn on with hard switching. I mean, we don't know whether it is hard switching or something, but we can say that it mostly goes through hard switching turn-on.

And the same thing will happen in the next half cycle when S2 and S3 suddenly turn off, and then after some time S1 and S4 turn on. At that time, the S1 and S4 may go for hard turn-on, and S2 and S3 will go for zero voltage turn-off. So, in summary, we can say that the S1, S2, S3, S4 are turned off with zero voltage, but S1, S2, S3, S4 are turned on with non-zero voltage or may or may not turn off. So, we can say with non-zero voltage, so we can say that this is a hard switch turn-on, and here it is we can say that soft or, you can say that since the dv/dt is limited, we can say this is a soft turn-off. So, we can say that here, I mean this thing with non-zero voltage, sorry, non-zero voltage. So, we can say that this condition may or may not. But in the worst-case scenario, we can take that they are turned on with hard switching.

So, we do not have control with this type 1 where the diagonal switches diagonal switches turn off simultaneously, we get, what happens is that the turn on instances, we may get a hard turn on or we can say that at worst case scenario, we always get hard turn on. However, during the turn off, the voltage across the, you know, the bridges or the voltage across the transformer winding

which is V_{AB} is limited by the slope. So, that is a, in summary, that is a type 1 PWM. Now, let us take type 2 PWM.

In type 2 PWM, Both the diagonal switches that means in this case we are seeing for S1 and S4. The S1 and S4 turns off at a different time. So here the turning off of diagonal switches at different times or you can say they are turning off in staggered manner one after the other so in this the initially again the same thing the S1 and S4 is in conduction so same thing the V_{AB} is nothing but in this case we have here you know V_{in} voltage is applied over here and we can say that the transformer current i_p is actually flowing through the L_{lkg}

And at the output we have the $i_L$current which is just an i_p will be nothing but the reflected current of this current i_L. Now in this case what happens is that now since we are going for turn off in a staggered manner or one after the other or you can say at different times. So, let us try to find for the leading leg. Let us try to first give the turn off of the switches in the leading leg. So, which is nothing but turn off of S1.

So here what happens is that here the S1 is turned off however the S4 is still on is still in conduction that is how we can create that the turning off at different times. So, because of that thing what happens is that since this is a L_{lkg} and this is your i_p current is there and this is your i_L current which is there. Because of that what happens, because of this i_p current in this direction, what happens is that the capacitor C1, C2, we can say the capacitor here is actually conducting in this direction and here it is conducting in this direction. If you see in the previous case, we can write V_{C2} is actually V_{in} voltage and V_{C3} is actually V_{in} voltage because S1 and S4 is on. in this case what happens is that since my S4 is still in conduction so we can say that my V_{C3} is actually still having the you know potential beam which will be coming over here this is C3 so in C3 however in this case we can say that the C1 is charging that means we can say V_{C1} is the voltage across V_{C1} is actually increasing from zero

and we can say C2 is discharging where V_{C2} is voltage is decreasing from vin voltage and this will continue until the voltage across $V_{C2} = 0$ and this voltage goes to zero at that point the

V_{C1} will becomes V_{in} voltage and at that point my diode D2 can turn on the diode D2 and here it is my diode D2 here it is D3 here it is D4 here it is this is my C4. So now let us take what happens because of this thing the i_p is flowing through through C1 and C2 and we can say that $i_{C1} + i_{C2} = i_p$ and i_p is nothing but the reflected current of the output inductor. Now, what happens? This continues until the $V_{C2} = 0$,because it is discharging and my V_{C1} becomes V_{in} voltage. So here C1, C2, C3, C4, D4, D3, D2, D1. Now here what happens is that Because of this thing my i_p current which is going through L_{lkg} is actually what happens is that this voltage is actually zero voltage and this voltage is actually we can say V_{C1} is actually V_{in} voltage. Because of this scenario what happens you can say that at that point the V_{AB} voltage is actually zero and we can say this state is nothing but a zero state because my $V_{AB} = 0$.

And in this case, my transformer current, you know, in this particular transformer current i_p , i_p can either, you know, we can keep it constant depending upon the current i_L which is there or if you want to make sure you can, you know, force this current to goes to 0 and stays at 0. So, at this point, you know, both the things are possible. If you want to keep it continuing, you can keep it continuing. Otherwise, because of the operation of the Circuit you can force this current to go to 0 because of putting some additional auxiliary circuit.

So, at this point to make the i_p goes to 0 and then stays at 0. Now, in this particular scenario, this particular system is called as the zero state. So, here V_{AB} voltage is actually going from V_{in} to zero volt, which was not the case in the previous case. If you recall, the V_{AB} voltage goes from V_{in} voltage to directly minus V_{in} voltage. However, in this case, the V_{AB} voltage, because of zero state, it goes from V_{in} to zero state.

And since it is going from V_{in} to 0 state, we can say that since it is going to V_{in} to 0 state, we can say that this is also sometimes called as the $+1$ state to 0 state. Now, since my D2 is on because of turning, turn on off. D2 because D2 is on the voltage across S2 switch the voltage across this switch since this is on is actually zero. So now when the gate pulse is given to S2 to

turn it on the S2 turns on with zero voltage similarly the case will happen when S2 and S3 is in conduction and S2 is turned off the C1 voltage discharges to zero D1 conducts and thus voltage across S1 switch goes to zero And now when S1 is given gate pulse, it will turn on with zero voltage. So, in a generalized case, we can say that the leading leg switches goes to soft turn on.

since the diode gets turned on before you are turning on the S2 switch before that it the diode turns on so the voltage across $V_{S2} = 0$ and we can say that the S2 turns on with zero voltage that means we can say that we have this soft switching of the S2 and here one more thing will happen here if you look very carefully since my S4 is on my vc4 value is actually 0 and since this is ON the entire V_{in} will come across the top device capacitance so we can say V_{S3} is nothing but equal to V_{in} then now after this what happens is you are. Now giving the turn off pulse to your switch S4 because you are, now in the lagging lag you are you are now switching thing from S4 to S3 you are going Already in the leading leg, we have already, you know, gone from S1 to S2 switch. And while going from S1 to S2 switch, we have seen that since our C2 gets discharged via this IP transformer primary current. Because of that, we have seen that the C2 gets discharged completely.

C1 gets charged completely to V_{in}. C2 gets discharged completely to zero. As a result of this, diode D2 conducts. and the moment that due to conduct so you turn on the S2 switch that's when you will get the gvs of pressure you can say gvs turn on of the S2 switch in the leading leg similarly i mean when the next switching comes in that means when it goes from S2 to S1 during that time S1 will go for zero voltage switching during turn on so what it indicates that in the leading leg we have we can easily get the soft switching because when the C2 is discharging to zero it is discharging using current i_p which is the reflected current from the if you recall it is a reflected current this one it is a reflected current from the output inductor and this current is enormously high you can say in in other words that this inductor is coming in series with this leakage and that's when the energy of that is pretty much higher so we will get our operation of this particular switch. So, we can say the C1 and C2 get discharged by i_p current which is which is the output inductance which is the reflected current of current of output inductor and since the reflected current of output inductor is enormously higher and this leakage this L_{lkg} and this inductor output inductor comes in series because you know since this i_L is the reflected current we can just write this we have you know $L_{lkg} + 1$ which actually gets shifted to you know primary side so you can say $\frac{1}{n^2}$ where n is nothing but $\frac{N_s}{N_p}$. So $\frac{1}{n}$ square times if let's say if the il current the average value of i_L current is the I_O which is going to output load. so, we can say half $i_p^{\ 2}$ and this energy is

large as L is generally a larger value and i_p is the reflected output current which is having a finite value so the condition to achieve softer known is that this

$$energy\ must\ be < \frac{1}{2}V_{in}{}^2C_1 + \frac{1}{2}V_{in}{}^2C_2$$

this is there and since since it is larger enough since it is large the leading leg switches will achieve the ZVS. Now if you look for the I mean in the lagging lag side when you know after the lagging lag switches it is changing its state that means from S4 now S4 gets turned off. Now during the S4 gets turned off what happens let's say D3 C3 D4 C4 during that time what happens because of this current i_p current which is there. Now this particular current will actually be flowing through this capacitance. So, there will be current which is coming over here and it goes in this direction and in the top direction.

So, this is also there. So, it will go and it will go in this direction. That means what you will see is that the V_{C3} is discharging. It is discharging. from you know a previous case it was vin and V_{C2} sorry V_{C4} is charging from zero volt and if you look very carefully the V_{AB}voltage since my S2 is completely on the V_{AB} voltage is

nothing but minus the voltage which is coming over here you know $-V_{C4}$ .You can take the loop in this particular you know in this particular loop if you take the loop it is nothing but V_{AB} and then this $V_{C4} = 0$, so this is nothing but vab it is nothing but equal to $-V_{C4}$. So and this $V_{C4}$is actually charging up the voltage is come is increasing since the voltage is increasing the V_{AB} voltage is actually we can say V_{AB} voltage is decreasing and it is decreasing and it is going to going to $-V_{in}$voltage because my $V_{C4} = 0$V, going towards V_{AB} voltage Now, because of this negative voltage applied across V_{AB}, the i_p, the current, i_p, current transformer, i_p, current will now decay, will now decay. Now, since it got decayed and it will no longer be, it will no longer be equal to, no longer be equal to, reflected output current this is I IELTS reflected output inductor current now because of that thing what happens is that i_p, will now decay and it will no longer be equal to reflected output inductor current and as a result of which what will happen is, you know, because of this thing, since this is no longer be equal to this i_p, so this

current has to find the pathway. That's when the DR1 and DR2 gets forward bias. Now, since DR1 gets, already it was forward biased, DR2 also gets forward biased. As a result of this, this entire winding gets short-circuited. Because this winding gets short-circuited, the voltage across this is actually 0.

And since the voltage across this is 0, this leakage will now be resonating with the C3 and C4. Now, in this case, what happens is that, however, because of the capacitor C3 and C4, we have limited $\frac{dV}{dt}$ at the output due to this charging and discharging of C3 and C4 by i_p, current.

$$\frac{dV}{dt} = \frac{C_3 C_4}{i_p}$$

and we can say that there is no reflected current from output inductor side so the energy associated with this current may not be sufficient enough to discharge this C3 and C4. So we can say that the energy which is there with this we can say that $i_p = \frac{1}{2} L_{lkg} {i_p}^2$ and this is this energy is there which is used to used to take out the energy from C3 and put in the energy into C4. It used to change the energy in, it used to change energy which is

$$energy\ in\ capacitance = \frac{1}{2} {V_{in}}^2 C_3 + \frac{1}{2} {V_{in}}^2 C_4$$

Now if load current is very less so that means my i_p will also be very less because you know i_p was the reflected current of i_L, So i_p will be very less that's when and already $L_{lkg} \ll L$, so the condition may be arises that this $\frac{1}{2} L_{lkg} {i_p}^2$ may not be greater than this particular energy that's when the C3 may not get fully discharged to 0 and C4 may not get fully charged to V_{in}, and that's when the S3 may go for you know hard switching they may not you know they may not you know they may not you know go through this the C3 may not achieve the zero voltage switching so this S3 may or may not so this S3 may or may not go to zero voltage turn on due to insufficient energy in you can say L_{lkg} okay energy due to insufficient energy due to due to i_p in a leakage since here this is output winding is fully short circuited my this side this side point is fully short circuited that's when there is no output inductor is coming in series with L_{lkg} and that's when we can say that my this the energy may not be sufficient enough to for the S3 to go through the zero voltage turn on so in this what we have understood that ZVS for lagging switch is difficult You know if the transformer current and the L leakage is not sufficient to discharge C3 to 0 volt and charge the C4 to V_{in} voltage.

This is the thing we understood in the Type 2 PWM, where the diagonal switches turn off at different instances. The leading leg switches will achieve ZVS because, along with L_{lkg}, this

output inductance will also come in series with this L_{lkg}, and that makes the combined energy of L and L_{lkg}. This is enormously higher because this $L \gg L_{lkg}$. L leakage will be in the range of tens of microhenry. However, this L could be in hundreds of microhenry. So, the energy associated when the L_{lkg} and L are in series is enormously higher.

That's when they can fully change the state of C1 and C2. That means they fully discharge C2. That's when we can get our D2 to turn on, and that's when we achieve the soft turn-on of S2 and achieve soft switching, or you can say achieving the zero-voltage turn-on of S2. S1 is relatively easier compared to S3 and S4, as in S3 and S4, we only have the L leakage and the transformer current, which is not the reflected current of i_L. That's when we may or may not get ZVS during turn-on.

Of the lagging switch. Because You know the Leakages are L_{lkg} value is very small.

So most. So, in the worst-case scenario. We will not get that. Zero voltage switching. So finally.

In the summary. If we do. You know. For type 2. If we do.

What we understood in type 2. The leading lag. Switches. Which is S1 and S2. Goes to zero voltage switching during turn on, or you can say during turn on, you can say soft turn on. Definitely soft turn on, and it is, I mean, it is definite even at the low loading condition also it will happen. However, the lagging lag switches S3 and S4 may or may not go go to zvs turn on okay so mostly you can say it is the hard turn on or you can say suddenly i mean when you're turning on the there is a some non-zero losses across this thing and dvdt is also not limited at the output of the lagging leg bridge however in this case and particularly this may not happens generally at low loading conditions at light loading conditions low or you can say light loading conditions mostly in light loading conditions and uh you know if if the L_{lkg} is very small. So, in both the cases this scenario happened and sometimes if these C3 and C4 output capacitance of devices are enormously higher and the voltage input voltage is enormously higher. So, during that time also it is not possible. So, this is the final understanding we got.

So, finally we understood that in type 1 when the in type 1 PWM when the type 2. So, we understood that in type 1 S1, S2, S3, S4 turns off with zero voltage switching S1, S2, S3, S4

turns off with zero voltage switching and they turned on without ZVS or you can say these are actually the hard turn on we get hard turn on of the devices so this is a type 1 when the diagonal switches are switching at the same time diagonal switches are turned off at the same time however in type 2 what we saw that the leading leg goes to you know zvs turn on always that means soft turn on and lagging lag depends upon depends upon the load and the leakage values and output capacitance and voltages it may or may not go to ZVS it may or may not go to ZVS turn on

However, if you look very carefully, in this case also, when, when, you know, in this case, when S4 turns off, they turn off with the limited $\frac{dv}{dt}$. So, we can say that they, they, you know, this S1, S2, S3, S4, they turn off with ZVS, you can say. Here also we can say the same way and in this one also when it is turned off because of C1 and C2, it actually turns off with the zero-voltage switching or you can say with the limited $\frac{dv}{dt}$ at the output of the half bridge or limited $\frac{dv}{dt}$ at the output of corresponding half bridges. here it is you know limited $\frac{dv}{dt}$ here it is not limited $\frac{dv}{dt}$ if you look here goes you know in the type 1 here it is not limited $\frac{dv}{dt}$ here it is with limited $\frac{dv}{dt}$ So, this is what you know the different PWM possibilities are there and one can select that required PWM and can able to achieve the you know required soft switching of the full bridge converter and thus can able to achieve nearly very less switching losses.

Even though you are going for a high switching frequency operation. And you need to go to a high switching frequency because you have an isolated transformer, and we know that the isolated transformer size is inversely proportional to the switching frequency. So, we go for a high switching frequency such that the size of the DC-DC isolated DC-DC converter is very small. Now, in the next class, we will study the phase-shifted full-bridge converter and its operation. Thank you very much for your patience in listening to this lecture.