CHARGING INFRASTRUCTURE

Prof. Apurv Kumar Yadav

Department of Electrical Engineering

Indian Institute of Technology Roorkee

Week-07

Lecture-32

Lec 32: Revisiting Isolated DC-DC Converters-III

Hello everyone, welcome to lecture number 32 of the NPTEL lecture series on charge infrastructure. In this lecture, we will see a full bridge-based DC-DC converter, obviously an isolated DC-DC converter. In this case, we have been discussing different isolated DC-DC converters, and in that, we have seen our forward converter. We have also seen various configurations of the forward converter. We have seen a forward converter with a unit demagnetizing winding, and we have seen a dual-switch forward converter. And we have understood the advantages and disadvantages of the forward converter. Then we moved ahead and saw the push-pull converter.

In the push-pull converter, we have seen how we can fully utilize the core by making sure the flux in the core goes from $- \varphi_m$ to $+ \varphi_m$, you know, value. That means we can go in two quadrants. I mean, the flux is going in a positive direction or in a negative direction. That's when we can ensure that we can utilize our core fully. That means we can allow the flux to go from $- B_{max}$ or flux density to go from $- B_{max}$ to $+ B_{max}$. Here in this case, we have only allowed it to go from 0 to B_{max} value, while here in this case, we went from minus B max to B max value. And for the same voltage, number of turns, and frequency, our area of core gets reduced by half. That means we can say we are fully utilizing the core. Now we have seen different disadvantages also with this push-pull converter, like the voltage kickback issue due to the leakage inductance of these windings. That also we have seen, and then we have seen that the switches have to be sized for twice the voltage rating. So those were some of the disadvantages we have seen with the push-pull converter. And then let us move ahead in discussing the other

DC-DC converter, most specifically the full bridge DC-DC converter, or you can say full bridge converter or commonly used full bridge converter. Now, in a full bridge converter, if you look very carefully, in full bridge, we are using two half bridges. Here we have designed our switch with MOSFET. One can also use IGBT with the body diode, but here we have the usage of MOSFET, which has some advantages. We will see that as we go along in this lecture and the next or subsequent lectures. We use the MOSFET so that we can go for very high frequencies.

And because of that, we will have some advantages. I mean, we can utilize some of the good advantages of this converter. So, let us see a simple operation. Since we have four switches, we can modulate them in different ways. So, we will see the first and simplest modulation.

We can say it is a full bridge-based isolated DC-DC converter. That is the most applicable. So, let us see the first simplest operation where, in my $\frac{DT_S}{2}$ period, I will turn on my S1 and S4 switches simultaneously. That means I am just turning on these S1 and S4 switches together. And if you look very carefully, this converter has two identical half bridges.

These are one half bridge. This is another half bridge, and from the pole of half bridges, we have connected the primary winding of this converter. The secondary part is similar to that of our push-pull converter. I mean, instead of this, we could have also done, you know, Ns number of turns. We could have done a simple full bridge. Rectifier, then C and R_L. Similar to that, we can do that. Instead of this rectifier power stage, we can just use this particular full bridge-based rectifier instead of a midpoint-based rectifier. Now, if you look very carefully here, we have DC, and because of switching these switches, we are actually injecting a high-frequency AC at the terminal of this primary winding of this transformer. On the secondary side, we are rectifying it and then applying it to the LC filter, which again has the same kind of architecture as that of the push-pull. We can also say that it is nothing but a derived buck converter topology. So now, if you look very carefully, let us see how this particular converter operates. It is called a full bridge because we have used two half bridges to make them work like a full bridge.

So in this case we are simultaneously turning on S1 and S4 switch. Since we are turning on simultaneously S1 and S4 switch we are actually applying if we define this as you know V_P voltage. So, from the V_P voltage we are actually applying Nothing but my V_{in} voltage, this S1

turns on, this S1 turns on and S4 turns on. That's when we are actually applying the V_{in} voltage across the primary winding.

Since we are applying positive voltage across primary winding, this side will now have $\frac{N_s}{N_p} * V_{in}$. This V_P is now $V_P = V_{in}$. during $\frac{DT_S}{2}$ period. because of that what happens is that this DR1 will get forward bias and since here again also we have

$$n \pm \frac{N_s}{N_p} V_{in} - V_o$$

Now reverse bias and then across L we are having I_L current, so V_L is

$$V_L = \frac{N_s}{N_p} V_{in} - V_o; \ n = \frac{N_s}{N_p}$$

This voltage applied across this inductor and since there is a positive voltage applied across inductor there is a positive slope of this thing which is nothing but $\frac{nV_{in} - V_o}{L}$, And since we are applying a positive potential across the primary winding, so the flux in the core will start rising linearly because, you know, $V = n\frac{d\emptyset}{dt}$, V is constant, n is constant.

So, $\frac{d\emptyset}{dt}$ is constant slope curve. So, we will start from $-\varphi_m$ and it goes to $+\varphi_m$ with the slope nothing but same as that of $\frac{V_{in}}{N_p}$. and if we see very carefully in this I_L current we have the average value of this I_L current is actually flowing through the load R_L while there is ripple component of that that ripple component is actually going through this capacitor I_C and that is what is drawn here that only the ripple part of that is drawn along the I_C current and since my S1 and S2 switch is on we are just having you know zero voltage applied across both the switches then in the next $(1 - D)\frac{T_S}{2}$ period what happens is that in $(1 - D)\frac{T_S}{2}$ period S1 S4 is off and since the S2 and S3 is already off here S2 and S3 is off here and here also S2 and S3 is off. So, we can say that since all the four switches are off we can say that this is off this is off this is off and since all the four switches are off if we assume that each switch has some output capacitance let's say C1 and C2 which comes because of the you know construction of the devices so this C1 and C2 the voltage will be appearing since all the four are off. So, the voltage in this part to this part will get equally divided among C1 and C2. Similarly, among C3 and C4, if in ideal case, if C1 and C2 are same and C3 and C4 are same. So, the voltage which is applied at this point is $\frac{V_{in}}{2}$ and here also $\frac{V_{in}}{2}$. So actually, there is no voltage which has been

imposed upon the V_p. And that's why we will see the $V_p = 0$ voltage is equal to zero since all the four switches are off.

And since it is voltage applied is zero the current which is going through there has to find a pathway so they will find a pathway going from top winding and bottom winding and since both because of that both the diodes will get forward biased both the diodes get forward biased and that's when you will see that the DR1 and DR2 is on that's when secondary bindings is completely short circuited so that's why we can say that we are now applying $+ \varphi_m$ or we are since short circuited then $\frac{d\emptyset}{dt} = 0$ is equals to zero since my $\frac{d\emptyset}{dt} = 0$ the $\emptyset$ will remain be the same at φ_m And since it is, you know, this both are forward bias, if you apply a KVL in this particular loop, we will get V_L to be equal to $- V_O$. You know, this voltage which is coming will come across this inductor, directly coming across this inductor. And that we will get in $(1 - D)\frac{T_S}{2}$ period, the same thing.

Now, in the next $\frac{DT_S}{2}$ period, what happens is that S2 and S3 is on while my S1 and S4 is off, is already off. Since my S2 and S3 is on, so we are now applying, if you see this one, we are now actually in this loop. and that's why we are now applying $- V_{in}$ voltage and since we are applying $- V_{in}$ voltage from V_P we are actually here on the secondary side we will see that our this potential is $- nV_{in}$ and here it is $- nV_{in}$ that's when you are now actually applying negative positive negative positive this is nv in voltage and that's when you will see that your DR1 gets reversed bias while your DR2 gets forward bias and because of that the I_L will be flowing like this coming back here like this And that's when we will see that the voltage applied across inductor.

If you take the KVL in this one $- nV_{in} + V_o$. So that will nothing but $v_L = (V_{in} - V_o)$. voltage applied across the inductor L. and again if we see this one this one is you know minus $- (1 - D)\frac{T_S}{2}$ and this one is nothing but $\frac{(nV_{in} - V_o)}{L}$. And then the ripple which is there will actually be flowing through the I_c. So that's why we have rising ripple , so we have rising ripple in previous duration it is falling so this falling part is actually going through the I_c while the average value is actually going through the load resistance and if we consider the previous case we have missed one point in $(1 - D)\frac{T_S}{2}$ period since my S1 and all the 4 switches were off and the C1 and C2 were blocking the half the voltages that's why they were having $\frac{V_{in}}{2}$ voltage if we assume both the switches to be identical in this case since my S3 and S2 switch is on. So, the

entire V_{in} will be appearing across S1 and in the second half duty will be appearing across S4 that's when the V_{S1} and V_{S4} is nothing but V_{in} voltage the voltage applied across the V_{S1} and V_{S4} is nothing but the V_{in} voltage.

So, if you look very carefully in this converter, we have to size our devices for only maximum up to V_{in} voltage. That is one advantage with this converter. if we see very carefully in $(1 - D)\frac{T_S}{2}$ period in that $(1 - D)\frac{T_S}{2}$ period we will see the same phenomenon will be occurring where what we will see is that our S2 switch and S3 switch is now off and all the four switches are off because already my S1 S4 is off and we can say that S2 and S3 is also off is also turned off since they are turned off what happens is that same thing will happen the zero potential applied across the primary and this inductor has to find the current the inductor current output inductor current has to find a pathway that's where it will start applying through the top winding and the bottom winding and that's when both the diodes will get forward biased and then the half of current will be divided into both the windings and as a result of which what happens is that from the inductor in this particular loop if you do it is just the $V_L = -V_O$ will be applied across the inductor, and in during that period since i have all the four switches are off and we assume that the switches are quite identical. So, the voltages will be appearing across their output capacitance equally that's when we have $\frac{V_{in}}{2}$ voltages which will be appearing across you know all the four switches and that is the thing we will see and since the voltage across inductor is $-V_O$, the inductor current is having negative slope of $-\frac{V_O}{L}$. So, we will see falling inductor current and the constant average value will be going through the resistance while the ripple value will be flowing through the capacitance. So, this is how we will see that we will get this particular analysis and when we do the and here also if you look very carefully just like in case of push-pull the inductor will see the ripple component which is nothing but two times of the switching frequency because in one T_S duration if the this is the entire T_S duration the inductor current repeats itself after every $\frac{T_S}{2}$ period. So, the inductor ripple frequency is nothing but twice the switching frequency and that's when we have to size our output inductor and capacitance to twice the switching frequency component So, the LNC has to be sized for $2f_{sw}$.

That is one advantage we will get with this kind of arrangement. Since the inductor current repeats itself after every $\frac{T_S}{2}$ period. So, we will now apply the volt-second balance in the $\frac{T_S}{2}$ period. So, we can now write You know, $V_{in} - V_O$ applied over $\frac{DT_S}{2}$ period $\pm V_O$ applied over

$(1 - D)\frac{T_S}{2}$ period, and it is equal to 0. That will give me the value $V_O = nV_{in}D$ which is what we got in the case of forward as well as push-pull converter.

However, here if you look very carefully, the flux is going from negative to positive Φm. So, that is when we are now utilizing the core fully. Also, if we look very carefully, the switching frequency or the frequency for which the inductor and capacitor have to be sized is $2f_{sw}$, or you can say the ripple component in the inductor is twice the switching frequency, and the voltage ripple across the capacitor is also twice the switching frequency. Now let us try to find how we can size the capacitor. Now, if you look very carefully in our previous discussion, we have seen that this inductor current ripple component is going through the capacitor. So, this value is nothing but ΔI_L because the ripple component is flowing through the capacitor. So now let us try to see the simplest thing, which is how we can size our capacitance.

So, this ΔI_L is only the ripple component of the inductor current, which is an AC current that goes between the maximum ripple value in the positive and negative direction. Now this ripple component of I_L is flowing through I_C. So let us try to see the sizing of capacitance. Now, if you look very carefully, C will have the ripple. Let's say the voltage across C is nothing but Δv_o. The ripple voltage is Δv_o, and that voltage is actually the amount of charge which has to be taken out or taken in from the capacitor, which will give us this Δv_o Now, in this curve, if we try to calculate our charge, at this time our charge gets into the capacitor, and in this time, it comes out of the capacitor. This much amount of charge, so we can take the area under this curve, this particular triangle, so we will get the area which is nothing but, since it is a triangle, this value is nothing but

going from this to this is nothing but $\frac{\Delta I_L}{2}$ and this ΔI_L is from this point to this point if we if we try to draw ΔI_L it is from this point to this point. So $\frac{\Delta I_L}{2}$ is in one direction, so it is half we can say $\frac{\Delta I_L}{2}$ And into this period, this period is nothing but if this is entire $\frac{T_S}{2}$, this is actually nothing but $\frac{T_S}{4}$. So, we can say into $\frac{T_S}{4}$. So, we can write the C value

$$C = \frac{\Delta I_L}{8 f_{sw} \Delta v_o}; f_{sw} = \frac{1}{T_S}$$

Now this is if you take our circuit, so this C has to be greater than this i mean if you define this as C critical. So, this $C > C_{cri}$, this value if you look here this value Δv_o is given in specification how much amount of ripple you can sustain fsw is the designer's choice.

okay and ΔI_L is something which you will allow the current ripple generally 5 to 10 percent of I_o . So that can be easily you know using this we can easily size our capacitance value in this full bridge converter. So, let us try to see how we can size our inductor as well If we look very carefully in this one, in $(1 - D)\frac{T_S}{2}$, we are applying minus V_o. So, we can write that

$$- V_o = L \frac{\Delta I_L}{\left(T_1 - \frac{D T_S}{2} \right)}$$

This we can write because we are applying in $(1 - D)\frac{T_S}{2}$, we are applying $V_L = - V_O$. So, thus we can write this one and then we can write as,

$$L = \frac{V_o (1-D)}{2 f_{sw} \Delta I_L}$$

And here if you look very carefully this minus sign we are just I mean that minus sign we can neglect because here the ΔI_L will be negative as it is going from maximum value of ripple to minimum value of ripple. So we can just take the magnitude or modulus of V_o as on the right hand side also we have taken only the magnitude of ΔI_L. so that's when we can rearrange and we can write L value in this way and this V_o we know that V_o value is

$$V_o = \frac{n V_{in} D (1-D)}{2 f_{sw} \Delta I_L}$$

If we look very carefully in this term this is generally 5 to 10 percent of i naught this is designer's choice and depending upon what could be the output voltage we can calculate this D depends on output voltage and number of turns N and this is again designer's choice N is designer's choice and this Vin is given in the specification Why I am saying designer choice because

depending upon what will be the you know V_{in} and V_o number of turns accordingly we can design that particular thing.

Now, so we have we understood how we can size our L and C and both L and C we see that we are designing it for 2 times plus w and that is why we can say that this L and C has to be sized for the frequency corresponds to twice the switching frequency. Now, this is the operation where what we are doing is we are turning on our S1 and S2 simultaneously for $\frac{DT_S}{2}$ period and we are turning on our S2 and S3 for $\frac{DT_S}{2}$ period and in $(1 - D)\frac{T_S}{2}$ period all the force which is we are turning it off. now if you look very carefully we can also derive the same thing you know another kind of converter which is nothing but the half bridge converter which is the performance i mean the most of the things will remain be the same let us define the half bridge converter in half bridge converter we have input voltage we have s1 switch S2 switch instead of having two half bridges with switches we can just have one half bridge with switches and one half bridge made up of capacitors you can have C3 and c4 and then midpoint we will take this this one on the other side if we just see this one on the other side we have this is np this is ns and this diode DR1 diode DR2 so this way RLC

And this is connected like this. Now, if you look here, we have V_{in} voltage and output is nothing but V_o voltage. And when we turn on here in this case, in this case, my S1 is on. And in this case, my S2 is on. And if you look very carefully across the C3 and C4, we have $\frac{V_{in}}{2}$ potential. $\frac{V_{in}}{2}$ potential is coming over here. And then if we look very carefully, In this circuit, whenever we are turning on S1 switch, so when we turn on the S1 switch, the V_{in} potential is coming over here. And in this loop, if we turn on this switch, then in this loop, we will get the potential, you know, V_p during $\frac{DT_S}{2}$. my vp is nothing but equal to you know $\frac{V_{in}}{2}$ you know this v in minus $V_{in} - \frac{V_{in}}{2}$ which is nothing but $\frac{V_{in}}{2}$, which is applied across the V_p and that V_{in} by 2 will be coming across this one here and if we say $\frac{N_S}{N_P}$ to be equal to N so it is nothing but N and Vin by 2 and that will be appeared across this inductor same operation as inductor and this inductor you know this VL is nothing but my N Vin by 2 minus V0

$$V_L = \frac{nV_{in}}{2} - V_o$$

if we do in this loop now in the next time when my already my S2 is off and when I turn off my S1 in $(1 - D)\frac{T_S}{2}$ period what happens is that across this one there is a output capacitance of

this switch So they will also be blocking this $\frac{nV_{in}}{2}$ and they are also blocking $\frac{nV_{in}}{2}$ as a result of which the voltage applied across this is 0 and since the voltage is 0 so what happens is that on the other side we have the current $I_L T_S$ going in this goes down on this side and this side and that's when we can say in$(1 - D)\frac{T_S}{2}$ period. it is nothing but $V_L = - V_o$ voltage applied , same as what we have seen in the full bridge case we are applying $- V_o$ and then if we do the same analysis you know our second balance balance on L if we do voltage across L we do that we will give

$$V_o = \frac{nV_{in}}{2D}$$

how we will write we can write here you know n v in by 2 minus v naught dt is by 2 and then minus v naught 1 minus D

$$L = \left(\frac{nV_{in}}{2} - V_o\right)\frac{DT_S}{2} + (-V_o)(1 - D)T_S$$

$\frac{T_S}{2}$ period equal to 0 and when we rearrange, we will get $V_o = \frac{nV_{in}}{2D}$.

And since we are, when we turn on this S1 switch, we are actually applying $\frac{V_{in}}{2D}$ from the primary winding. So, that is why we have $\frac{V_{in}}{p}$ with that our flux will be rising. It reaches plus 5 M and then when my S1 switch is off, my S2 is already off. So here S2 is off. S1 and S2 is off.

Here my S1 is off. S1 and S2 is off. So during that time, both the S1 and S2 is off, the Vp applies 0, and that's when the current will be distributed among the two windings, and that's when we can say that these two windings are short-circuited, Vp is equal to 0, that's when my d phi by dt is equal to 0, that's when my flux is actually constant term, which is plus phi m. And since that the current because of that my VL applied is $- V_o$ the current will be falling down.

Here it is n Vin by 2 - $\frac{V_L}{2}$ value it is going to be minus V0 L it is falling down.

And when we see that whenever my S1 switch is on, the voltage is 0 across the S1 switch. When my S1 switch is, you know, during this time when it is off, the capacitor of this device, the output capacitor of devices, will have equal voltages applied across them, which is nothing but 2. And whenever the S2 switch is on during another next $\frac{DT_S}{2}$ period, the entire voltage will come across S1, and that's when S1 has to block. Voltage, so it is similar to that of the full bridge except for two things: one, the output voltage is actually reduced by two because we are now using just one half-bridge; another half-bridge is made up of a capacitor, you know,

series-connected capacitor. So, we have reduced the DC bus utilization, or you can say the DC utilization, by half. The voltage, however, we do not now use four switches; we just have to use two switches and two series-connected capacitors. So, this is all about the full-bridge and half-bridge converter. This full-bridge converter, you know, when both the S1 and S4 switches are operated diagonally, you know, together, and S2 and S3 switches together diagonally. So, we will see you in the next lecture. Thank you.