

CHARGING INFRASTRUCTURE

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Week-05

Lecture-24

Lec 24: Three Phase AC-DC Converter-II

Hello everyone welcome to the lecture number 24 of this NPTEL lecture series on charge infrastructure and in this lecture we will carry forward our discussion on three-phase ac to dc converter if we recall of what we discussed in the last lecture so we saw that what's converter look like three-phase ac to dc converter which is also called as the front-end converter also called as the active rectifier we can say now in this we have we are using identical three half bridges and having through the pole we have connected the inductance L and then to the source 3 AC source having phase difference of 120° and then we have a capacitor and this entire converter is feeding to the load R_L and we have seen the operation of this so we understood that we can control the current which is going into this one by ensuring the voltage across the inductors in a proper manner that means this side voltage from the source is constant. However from the other side we can apply the variable voltage at a variable phase angle with respect to this source voltage and that's when we can ensure that there is a current flow either from this source either from the ac source to the converter side or from the converter side to the ac source side so here we can see that whenever there is a power flow which has to be taken place from the ac source to the converter side we will apply the voltage through the converter at an phase lag of δ and in that case we ensure that the current is being drawn from the source to the converter and following the unity power factor current however when we talk about the backward power flow that means from the dc side to the ac side

we can ensure the phasor from the converter is actually leading the phasor corresponds to the voltage source by a required angle δ . And by changing the value of this δ , we can ensure the current which is going from one AC source to another AC source. We can control the

amount of current which is going from one AC source to another AC source. And this particular thing we are talking about we have only draw this particular phasor for the fundamental frequency component or you can say for the fundamental frequency that means our frequency of contention is actually nothing but the line frequency or the frequency of the AC signal. And then we understood the operation after understanding the operation we have derived the inductance value which has to be corrected in series with all the three source and in this we have understood this the value of the inductor should be this much and here if we see 'm' is nothing but the modulation index now that modulation index is the designer's choice and they can select the value and mostly it will be between 0.8 to 0.9 Similarly, the $v_{s,pk}$ is given in the specification which is nothing but the peak of the AC voltage source and here we assume that we have the balanced operation where all the three phases are loaded equally and then here if you see V_o is again given in the specification table because generally in the specification they will mention the output power, output voltage and the information related to the grid side related to the input voltage input frequency similarly here is the line frequency also given in the specification. You know it's a designer's choice and then the $i_{s,pk}$ you can easily predict from the specification table because we know what is our load power so we can say this is PL and it is for the three phase, so divided by three that is a per phase and we have the v phase rms and this will nothing but gives the my current in the rms value multiplied divided by $\sqrt{2}$, when we do we will get the isp value and that we can put it over here this is assuming assuming no loss in the power converter in other case you can also take some efficiency term so we can write I mean and that efficiency term we can write it in the in the denominator we can write some estimated efficiency, let's say some eta we can take eta of the converter if we assuming no loss then we can just take our this relationship to calculate the isp and from there we will calculate the L and once we know the L value we must ensure that the voltage drop across inductor obviously in i mean corresponding to fundamental frequency must be less than 10% of the input peak voltage. That means you can say that $\omega L i_{s,pk}$. That the voltage drop has to be less than 10% of $v_{s,pk}$.

And if you are not getting that, then you again come here and change this value of 'm' modulation index. Maybe increase the modulation index and that's when we can able to ensure that the L value changes and that's when $\omega L i_{s,pk} < 10\%$ of $v_{s,pk}$. This condition has to be

ensured. Otherwise, if there is more voltage drop, then the maximum voltage will be dropped across the inductor. So, that is why m has to be calculated accordingly.

Now, after this, let us move ahead and understand how we can size our switches. So, you can see sizing of switches. Now you can recall our discussion in the PWM lectures that means lecture number 22 where we understood that when we have taken the half bridge converter we understood that the duty ratio for which the switch has to be on is given by $1/2 + \left(\frac{v_m}{2V_c}\right)$ and here we know that our modulator this is again modulating signal and this is our carrier signal I mean this we get it from discussions in lecture number 22 so in case of we can write in case of sine pwm or spwm sinusoidal pwm We can write, so sinusoidal PWM means our V_m is nothing but $v_m \sin \omega t$. Modulating wave is having the $\sin \omega t$ variation. So, we can write as $+ \frac{v_m \sin \omega t}{2V_c}$.

And that will be nothing but D will be

$$D = 1/2 + \frac{m}{2 \sin \omega t}$$

where m is nothing but V_m/V_c . And this is the duty ratio if you have taken, I mean, if we take just the half bridge. This is here in this case; it is V_o . Now we have the inductor and we have the source, and assume this source with respect to the fictitious inductor.

I mean this fixed voltage, so that I can write using this fictitious 'o', and this is with respect to fictitious 'o'. If we take the fictitious midpoint 'o', we take this one. So this is A. I have I'm only taking one of the half bridges because we assume that it's a balanced operation of the converter, so all three phases will also follow the same pattern, obviously with a 120° phase difference. So now what we see is that this duty ratio of S1 is defined by

$$D = \frac{1}{2} + \frac{m}{2} \sin \omega t$$

and we will switch the S2 switch for 1 minus. So, this is for the S1 switch, and for the S2 switch, it is 1 minus d , and that is nothing $D = \frac{1}{2} - \frac{m}{2} \sin \omega t$

now if I have to size these switches if let's say these switches are made up of MOSFETs if MOSFETs is used in MOSFETs with body diode is used And we ensure that whenever there is conduction through the body diode, we will turn on, we will form the channel through the MOSFETs.

So, the current will start flowing through the channel. So that's when we have to define the RMS current which is flowing through the MOSFETS. And for that, we have to calculate the IRMS. So we can say IRMS of S1 is nothing but we can write down $1/T$, going from 0 to T.

We can write, you can see D, and we assume that the current drawn from the source is nothing but $I_{spk} \sin \omega t$ same as that of V_a , which is nothing but $V_{spk} \sin \omega t$ of a phase or source voltage.

So, we have D times my current, which is $(I_{spk} \sin \omega t)^2 dt$. You can write this, and this one we can put it as :

$$I_{rms,S1} = \sqrt{\frac{1}{T} \int_0^T D \cdot (I_{spk} \sin \omega t)^2 dt}$$

$$I_{rms,S1} = \sqrt{\frac{1}{T} \int_0^T \left(\frac{1}{2} + \frac{m}{2} \sin \sin \omega t \right) \cdot (I_{spk} \sin \omega t)^2 dt}$$

This you can solve to obtain your RMS current flowing through the switches, through the switch S1. Similarly, you can also calculate the $I_{rms,S2}$, which is as:

$$I_{rms,S2} = \sqrt{\frac{1}{T} \int_0^T \left(\frac{1}{2} - \frac{m}{2} \sin \sin \omega t \right) \cdot (I_{spk} \sin \omega t)^2 dt}$$

So, one can solve these two equations and can calculate your RMS current through the switches. If the switch is realized using MOSFETS with body diode, realize S1 and S2 switch. And then, in the same way, S3 and S4 and S5 and S6 will be there. Now, similarly, if let's say the S1 and S2 switch is realized using IGBT with freewheeling diode—using IGBT with freewheeling diode—now, if this switch is realized using IGBT with freewheeling diode, then we can draw our one of the half bridges something like this. We have switch S1, and since the freewheeling diode is placed across the IGBT to allow the current in the negative direction, we have placed a diode D1. Similarly, we also have the S2 switch and the freewheeling diode D2.

Now, this is having plus and minus voltage V_o , and that we can just take the fictitious O point and then connect our grid and inductor in this manner. This is nothing but $V_{spk} \sin \omega t$. Now, here we assume that, as you know, we are assuming that our converter is operating with unity power

factor. So, we have UPF operation, and for now, for you know, for easy calculation, let us assume that the current is now being coming out of this half bridge. So, we can just define this $I_{spk} \sin \omega t$ as we have the unity power factor operation.

So, if you look very carefully, when in this half bridge, when the S1 device is on, let us say during the positive half cycle, the current is going from the collector to emitter terminal of the switch S1, which is IGBT. However, during $(1 - DT_s)$ period, when the switch S1 is turned off and switch S2 is turned on, because of the direction of current, it will start flowing through the diode D2 and then it will flow back to the source. And let us see if in case of a negative cycle, when the current direction is in negative, And the current direction is in this way. So, however, in the negative half direction, when the current direction is this way, whenever the S2 switch is on, the current will flow through the switch S2, that means between collector to emitter.

While when this S2 switch turns off, then the current will start flowing through the device D1 or you can say through the diode D1. So, we can write, We can write in positive half cycle, if we assume the current direction in this way in positive half cycle, when your $v_s > 0$, we can say that our switch S1 is in conduction for DT_s period. Whenever the switch S1 is turned on, the current will start flowing through this switch S1 between collector to emitter because we assume that current is coming out of this pole of this half bridge.

While when the switch S1 is turned off, that means in $(1 - DT_s)$ period when the switch S1 turns off, So, because of the direction of the current, since it is coming out of this pole of the half-bridge, this diode D2 will turn on, the current will start flowing through the diode D2 automatically. So, as a result of which the diode will be conducting in $(1 - DT_s)$ period. And if we see in the negative half-cycle, when $v_s < 0$ is, what we will see is that when the, you know, when the S2 is turned on for during the 1 minus GTS spread, the current will

Because the current direction will now be going into the half bridge, it will go through the S2 switch. And when the S2 switch turns off, that means during the DT_s period, so when the S2 switch turns off, the current, because the current direction is coming into the half bridge, it will start flowing through the diode D1. So, we can say that in the negative half cycle, the S2 switch,

which will be there, will be on for $(1 - DT_s)$ period. And the D1 diode will be turned on for DT_s period because of the current direction. They are in conduction.

And our $T_s = 1/f_{sw}$, which is switching frequency. So, now if we look very carefully, the switch S1, if you see the switch S1, the S1 switch is in conduction for DT_s duration where the D what we have already know from the previous slide is

$$D = \frac{1}{2} + \frac{m}{2} \sin \omega t$$

and this particular is in conduction for DT_s period during the positive half cycle only during the positive half cycle. And or you can say the D2 diode is in conduction for $(1 - DT_s)$ period and duration. And this is again during positive half cycle. And so, we can write, so we can easily do $1 - D$, we will get

$$(1 - D) = \frac{1}{2} - \frac{m}{2} \sin \omega t$$

And this if we take in a general sense because the switch S1 will only be conducting in the positive half cycle while in the negative half cycle it will be completely off. So, we can write in a simpler manner that $I_{avg,S1}$ of switch particularly we will write for S1 is

$$I_{avg,S1} = \frac{1}{T} \int_0^{T/2} \left(\frac{1}{2} + \frac{m}{2} \sin \omega t \right) I_{spk} \sin \omega t dt$$

$$I_{avg,S1} = \frac{1}{T} I_{spk} \int_0^{T/2} \left[\frac{1}{2} \sin \omega t + \frac{m}{2} \sin^2 \omega t \right] dt$$

$$I_{avg,S1} = \frac{I_{spk}}{2\pi} \left[1 + \frac{\pi m}{4} \right]$$

So, with this, you know, one can easily calculate what is the average current going through the switch S1. Similarly, we can now define the IRMS. Switch, I mean for S1,

$$I_{rms,S1} = \sqrt{\frac{1}{T} \int_0^T D \cdot (I_{spk} \sin \omega t)^2 dt}$$

$$I_{rms,S1} = \sqrt{\frac{1}{T} \int_0^T \left(\frac{1}{2} + \frac{m}{2} \sin \sin \omega t \right) \cdot (I_{spk} \sin \omega t)^2 dt}$$

$$I_{rms,S1} = \frac{I_{spk}}{2\sqrt{2}} \left[1 + \frac{8m}{3\pi} \right]$$

So, this is the RMS current which is going through the switch S1.

Similarly, you can also take the, you can also calculate the average current for the diode as well. $1/T$, 0 to $T/2$, is $(1 - D) I_{spk} \sin \omega t dt$. And this, when you solve, you will get $1/T$. And this, finally, when you solve this thing, you will get the expression

$$I_{rms,S1} = \sqrt{\frac{1}{T} \int_0^T D \cdot (I_{spk} \sin \omega t)^2 dt}$$

$$I_{avg,D2} = \frac{1}{T} \int_0^{T/2} (1 - D) \cdot I_{spk} \sin \omega t dt$$

$$I_{avg,S1} = \frac{1}{T} \int_0^{T/2} \left(\frac{1}{2} - \frac{m}{2} \sin \sin \omega t \right) \cdot I_{spk} \sin \omega t dt$$

$$I_{avg,S1} = \frac{I_{spk}}{2\pi} \left[1 - \frac{\pi m}{4} \right]$$

$\left[1 - \frac{\pi m}{4} \right]$, which is, you know, this is plus here, it is minus, and then you can calculate I_{rms} . I mean, you can also calculate that $I_{rms,diode}$ going through a diode, especially for diode D2. D2 is

$$I_{rms,D2} = \sqrt{\frac{1}{T} \int_0^{T/2} (1 - D) \cdot (I_{spk} \sin \omega t)^2 dt}$$

$$I_{rms,D2} = \frac{1}{T} \int_0^{T/2} \left(\frac{1}{2} - \frac{m}{2} \sin \sin \omega t \right) \cdot (I_{spk} \sin \omega t)^2 dt$$

$$I_{rms,D2} = \frac{I_{spk}}{2\sqrt{2}} \sqrt{\left[1 + \frac{8m}{3\pi}\right]}$$

This is I_{rms} of diode D2. So, if we use the IGBT with freewheeling diode, then the switch S1 has to be rated for this RMS value of current, and the diode D2 has to be rated for this value of RMS current. Similarly, the average current of the diode, the freewheeling diode D2, should be defined by this expression, and the average current through the IGBT S1 will be of this particular expression. And similarly, you know, if you can also derive for S2 and D1 by putting the appropriate values of limits of integration and duty ratio values, and that's when, you know, by following these particular expressions, one can easily able to predict what will be the, RMS and average current ratings of freewheeling diode and the switch, which is an IGBT. And here, you know, this I_{spk} you can easily calculate from the specification, as we have already told previously, and thus one can easily define the current ratings, and that's when one can actually, you know, select the devices accordingly.

Similarly, we can also say the voltage stress across the devices. The voltage stress across devices. Because S1 and S2 if we look very carefully. Let's say this is we are drawing with very V_o . And this is a fictitious point 'o'.

So it is $V_{spk} \sin \omega t$ this is 1 and if we see the S1 and S2 switch so when the S2 is on if the entire voltage V_o is appearing across the S1 and when S2 switch is on the entire V_o is coming across S1 so we can say that the voltage across this one is nothing but the V_o and we are actually to provide the safety margin with the voltage rating of S1 and S2 switch will be nearly we can take 1.4 times V_o where 40 percent is nothing but the safety margin now this safety margin has been taken because this output voltage will also have some ripple over this at the same time when you switch off one of the switches there the parasitic inductance will come into picture and that's when when you switch off the voltage the switch the voltage across the switch will look something like this Where this is nothing but the V_o and this is due to parasitic inductance of the loop. This is the voltage across which is S1 and S2. Now, this we know that let us say the L parasitic is the parasitic inductance.

So, this voltage drop is nothing but $\frac{dI}{dt}$. So this will appear across the switch which is actually turning off and that's why we have to size our switches for that safety margin and that's why we take generally 40% or 30% of the safety margin. Now if we look our converter, let us look back our converter. If we look our converter, we have actually derived the L value, inductance

value or the RMS current going through the inductance we have already discussed in the last class. We have derived understood the voltage and current ratings of the switches now the next component is the capacitance now let us do the after knowing our inductance value switches rating let us also do the sizing of this capacitance. So first let us do the sizing of capacitance In this sizing of capacitance let us first try to find as in the case of single phase ACVDC converter where we did the power balance and from the power balance we understood that the single phase ACVDC converter we have second line harmonics component on the voltage ripple of the capacitance. Now let us see what will happen in this particular case when we do the same procedures here. So, when we do the same procedure, we can say that the output power we can say that it is nothing but your V_o multiplied by let us take the power which is coming at that point. So, here the voltage same voltage will be there, but the current is nothing but I_{conv} .

And we can also say that our input power, again output power I am talking about here, between A point and B point at AB terminals. So, input power is nothing but, if we have three-phase signal, we can say $V_{spk} \sin \omega t$, $I_{spk} \sin \omega t$ again we assume that we have the unity power factor operation plus again assuming upf operation so this is the power at through the a phase similarly we can write power at b phase and power at c phase this is summing up and that is nothing but equal to nothing but equal to the input power and now through power balance if i mean if there are no losses in converter there is or if there is lossless converter that means whatever power which is coming from here is actually equal to the power at that point . So we can say apply power balance that means input power equals to output power obviously this we are saying

instantaneously as well as the average power and that's when we can say that

$$V_{o, conv} i_{conv} = V_{spk} \sin \omega t \cdot I_{spk} \sin \omega t + V_{spk} (\sin \omega t - 120^\circ) \cdot I_{spk} \sin(\omega t - 120^\circ) + V_{spk} (\sin \omega t - 240^\circ) \cdot I_{spk} \sin(\omega t - 240^\circ)$$

$$V_{o, conv} I_{conv} = V_{spk} \sin \omega t \cdot I_{spk} (\sin^2 \omega t + \sin^2(\omega t - 120^\circ) + \sin^2(\omega t - 240^\circ))$$

$$V_{o, conv} i_{conv} = V_{spk} \cdot I_{spk} \left[\frac{1 - \cos 2\omega t}{2} + \frac{1 - \cos(2\omega t - 240^\circ)}{2} + \frac{1 - \cos(2\omega t - 480^\circ)}{2} \right]$$

$$V_{o, conv} i_{conv} = V_{spk} \cdot I_{spk} \left[\frac{3}{2} - (\cos 2\omega t + \cos \cos(2\omega t - 240^\circ) + \cos \cos(2\omega t - 120^\circ)) \right]$$

The $\cos \cos(2\omega t - 120^\circ)$ and this term this entire term is nothing but equal to 0 at any given instance of time so we can say that $V_{o, conv} i_{conv}$ is nothing but we see that

$$V_{o, conv} \cdot i_{conv} = \frac{3}{2} V_{spk} \cdot I_{spk}$$

$$i_{conv} = \frac{3}{2V_o} V_{spk} \cdot I_{spk}$$

Now if we see there is absence of that indicates there is absence of there is no second line frequency component. So there is absence of second line frequency component. So if you look very carefully in this converter this particular current has only the DC component and there is no second line harmonic component there is no third there is four there is not no lower order harmonic component in this i_{conv} current and only the high frequency currents will be there in this i_{conv} current we because in this particular derivation we have only take line frequency component of the current and we know that during the operation along with this line fundamental frequency component we are also having the you know high frequency component voltage component are also there. So that is when you will have high frequency current as well. So we can say that here there is no there is absence of second line harmonic component only dc component exist , only DC component exists. There is no second line frequency component. In case of single phase converter, we have the second line frequency component and that is the reason why we could not take three single phase converter. Instead of taking three single phase converter, we have taken the three half bridge based converters and we are making them operate in a balanced three phase manner.

So that is the reason why This will result in small capacitor size for 3 phase AC to DC converter. Which was not the case when we will use 3 independent single phase AC to DC converter as all the 3 single phase converters will have the second line harmonic voltage ripple at the output capacitor thus require 3 large capacitors to keep the output voltage ripple within the limits. So that is the reason why the three independent single phase converter is not preferred instead of that single three phase converter with three half bridges operated with 120° phase difference is being used. And when we do that we ensure that there is no presence of second line frequency component in the i_{conv} current and that's when there is no second line harmonic component in the capacitor voltage. now what would be the next frequency component which will be present in the i_{conv} because that frequency component will be flowing through the capacitor and the dc will be going through the output load so let us try to see what would be the

component of current which will be present in this i_{conv} current so we know that for the fundamental frequency we have drawn.

Fundamental frequency: we have drawn the equivalent circuit, single-phase equivalent circuit, to be like this, where here we have $V_s(t)$, L and we have v_{conv} , R (I mean with respect to time t), and we have current I_s . Now, we know that our v_{conv} has fundamental. From Lecture 22, our average variation of pole voltage is nothing but the fundamental frequency component, along with harmonic frequency components at sidebands of mf . Which is nothing but mf is nothing but my f_c/f_m , or you can say that fundamental frequency. And here, our fundamental frequency is our line frequency. So, in this case, what we see is that $v_{conv}(t)$ has a fundamental component, and along with that, we have harmonic components.

So, when we draw this for the fundamental frequency, this is the single-phase equivalent circuit. So here, we have seen that because of the fundamental frequency component, there is no introduction of harmonics in i_{conv} , and thus there is no ripple on the output capacitor voltage. It is just the DC quantity. So, let us see what will happen when we draw the circuit for harmonic frequency components. So, for harmonic frequency components, the single-phase equivalent

Equivalent circuit will look like this: if you see, since the source is a pure AC source, there is no harmonic frequency component, so the source will be short-circuited while we have this L , and along with that, we have our component, which is nothing but v_{conv} where n or $v_{conv}(n)$, where n is the harmonic component, and that harmonic component will be at the sidebands of mf , which are sidebands of the carrier frequency. So, what we have is a circuit like this. Now, because of this circuit, there will be current through this circuit. I_s of that particular frequency component. So, we can say that $I_s(n)$ is nothing but $v_{conv}(n)$. Let's say, if it is with respect to t , we can say with respect to t divided by here. Now, this impedance L will not now be n times w , which we have as $n \cdot \omega \cdot L$, where ω is nothing but $2\pi f_m$, or here our f_m is nothing but our line frequency. So, we can say w is nothing but $2\pi f_s$.

So, what we see is that because of the fundamental component, we have the component of current which is having the fundamental component. So, the current will have the fundamental

component which is nothing but we assume to be having a utility power factor current. So, it $I_{spk} \sin \omega t$ which we obtain over here and because of the harmonic frequency component so because of that what we have harmonics along with this pure sinusoidal current.

We also have the harmonics current and that harmonic current will actually introduce harmonic component of current in the I converter and that will be harmonic current has to be filtered out by capacitor C while the DC current will be going through the load RL. So, what we understood in the case of fundamental frequency component for the fundamental frequency component the equivalent single phase equivalent circuit will be having we have the I_{spk} and we have the ωL impedance and then we have the v_{conv} , I mean here again it is $j\omega L$ and here we can also say it is $j\omega nL$ and here again we can say it is $j\omega nL$ and that corresponds to the current which is nothing but $I_{spk} \sin \omega t$ because we are assuming that we have the unit power factor operation. So, that current is the fundamental component of current. However, along with this fundamental component, we also have the harmonic current and that harmonic current is happened because

The output of the half bridge which is you know the pole the average pole voltage variation has the fundamental component and along with that it has the harmonic component which is at the side bands of mf or side bands of you can say the carrier frequency which we have studied in lecture number 22 and that is when we can see that This harmonic component of current will result in the presence of harmonic component in I converter which corresponds to the AC component of current which is flowing through the capacitor. And that we will derive in the next class to understand the RMS current rating of the capacitor bank and then we will see how we can calculate the value of capacitance afterwards. So, thank you very much for listening to this lecture and we will continue our discussion on how to size our capacitor bank because the capacitor bank is very important because in here in case of single phase what we have understood we understood is the dominant component of current which is going through the capacitance is the second line harmonic component and that's when we design the capacitance corresponding to that second line frequency second line frequency component but here in this case in case of three-phase converter that there is no

The second line harmonic component of current in the I converter current, and that's when there is no second line harmonic component of voltage or ripple on the capacitor. It will only have a high-frequency component of current. I mean, the I converter only has the high-frequency component of current, and that value of current will flow through the capacitor, which will correspond to the ripple in the capacitor. However, that harmonic component of current has a lesser amplitude, and we will see in the next class how that current will look. And then, from there, we will solidify our understanding of the sizing of the capacitor bank. Thank you very much for patiently listening to this lecture.