

CHARGING INFRASTRUCTURE

Prof. Apurv Kumar Yadav

Department of Electrical Engineering

Indian Institute of Technology Roorkee

Week-04

Lecture-19

Lec 19: Totem Pole PFC Converter-II

Hello everyone, welcome to the lecture number 19 of this NPTEL lecture series on charging structure. In previous lecture we have discussed about totem pole PFC, we will continue our discussion in this lecture as well. So, let us see what we have understood as of now. We understood that this totem pole PFC is nothing but a derivative of bridgeless PFC where we do not have any diode bridge rectifier at the first stage.

And we have here we have also understood that in this S1 and S2 switches are the ones who are switching at a very fast switching frequency $f_{sw} > f_s$, which is far greater than line frequency f_s , and while the diodes are actually being I mean, it is on for one half cycle, while the other half cycle it will be off. So, diode switching with the line frequency while the switches are switching at a high switching frequency. So, this we can easily take it in a form like we can also use a switches as well having a free willing diode or the body diode if we use mosfet so we can also realize this converter having four switches and all the four switches S1 and S2 are switching with a high switching frequency f_{sw} which is very very much higher than the line frequency while the S3 and S4 are switched only once in a line cycle so they are switching at a very slow switching frequency which is f_s same as the line frequency and in one line cycle we have several or so many switching cycles depending upon how much times the f_{sw} as compared to f_s . Similarly, we have also seen the rms current of S1 switches which is shown over here here we have this we can easily put i_s is

$$i_s = I_s \sin \omega t$$

We assume that this converter is drawing unity power factor current from the source and we can also know that we also have this inductor and capacitor so this inductor and capacitance value is same as that of

of boost PFC converter where R_L indicates the load power, f_s is nothing but the line frequency component, and ΔV_o is the allowable voltage ripple on the capacitor, and V_o is the output voltage. At the same time, L is nothing but V_o divided by $4 \Delta i_L$ or $\Delta i_{L,max}$, which is the maximum allowable current ripple times $f_{s\omega}$.

$$L = \frac{V_o}{4\Delta i_L} = \frac{V_o}{\Delta i_{L,max}}$$

And if we look very carefully, this capacitor, since it is having a single-phase power factor correction converter, having the unity power factor current drawn from this input source, so this capacitor will have second line harmonic component on its voltage. So, output voltage has the second line frequency component of voltage riding over the DC value V_o . Now let us see as in the case of boost PFC where our control objective was to have the output voltage getting regulated at the same time making sure the average current which is being drawn from the source is nothing but having the unity power factor.

So both the things has to be ensured while doing the closed loop control. So let us try to see how the closed loop control look like. Again in the closed loop control it is we are again we are here we are trying to do the closed loop control of average current flowing through the inductor and here the average current flowing through the inductor is nothing but same as that of the current which is been drawing from the source. So, if we can ensure that the average current flowing through the inductor is having the sinusoidal variation and having the phase angle same as that of the AC voltage. So, we can ensure that the i_s current or the grid current which is being taken is also having the unity power factor variation.

So, here what we do is again our main requirement we will define the reference voltage whatever reference voltage we want we will do the summation of that send it to the voltage

controller, this voltage controller will be output of this voltage control will be clamped to the maximum allowable current in the converter, because before doing the closure control we would have already selected the devices having the required currents so we have already defined that rating so that's why the clampings are needed and that will be sent to a multiplier block. Now if you recall in case of boost PFC we have multiplied the output with modulus of unit $\sin \omega t$ but here we will multiply it with the unit \sin which is just unit $\sin \omega t$. Generation of this unit $\sin \omega t$ is critical in order to ensure that the current drawn from the source is having the same frequency component as that of line frequency and also having unity power factor operation.

It is because our grid voltage have small variations in frequency around the nominal value that means 50 Hz or 60 Hz, and also have harmonics in it. So, we need to track these small variations in frequency to accurately detect the zero crossings and matching the $\sin \omega t$ which is difficult things to do. There are a lot of literature available addressing this problem using advanced phase lock loops and filters. However, in this particular laxative we are not discussing that

Here we can assume that we can just sense this voltage, grid voltage and we can just divide it by the peak value of the voltage which we are obtaining and that we can directly multiply it with the current reference which we are meaning the magnitude which we are getting at the output of the voltage loop. And this is nothing but will define the $i_{s,ref}$ you can say the current which we are getting over here because our i_L is nothing but is and again it will be compared with this comparison we will take down from the circuit. So it is nothing but the i_s , so we can take from here and that i_s then send it to current controller again output of current controller is sent to gain k_i block and that will be sent to the modulator block does nothing but calculate the duty ratio or the whatever duty ratio is coming and then depending upon the the grid voltage whether it is in the positive half cycle or negative half cycle decide the switching of this switches like whether it should be d or whether it should be $1-d$ accordingly, these two switches will be defined. While if $v_s > 0$, you are that means positive half cycle S4 is on if it is in negative half cycle S3 will be equal to 1. So, here you will get the PWM for PWM_{S1} , PWM_{S2} , PWM_{S3} and PWM_{S4} you will

get. And this output which output voltage what you are having this you can sense and you can feed it back to the reference voltage similarly whatever current feedback we are we are seeing we can take sense it and using the current sensor and send it back to the loop. So, here we have is feedback here we have we not feedback

And again as we have derived those closed form solutions or we have defined the $G_i(s)$ or $G_v(s)$, here also the same way we will also obtain the same $G_i(s)$ and $G_v(s)$, and then we can you know we can design our controllers following the steps what we have what we have seen in case of boost PFC case. And using this method we could be in a position to to basically ensure that whatever we are having the unity power factor current turns on the source at the same time we are maintaining the voltage at a reference value now if we talk about modulator block so the input of the modulator block is nothing but d duty ratio d which is varying with T so that we can again pwm S1 can be generated in similarly i mean here in the modulator block we also need to sense we can also sense this voltage And we can send it to this modulator block. Similarly, we can actually send it to this unit $\sin \omega t$ block generation. And we can use the same thing to generate the unit sine waveform or $\sin \omega t$. Now, here if we look very carefully, why we are taking this?

Just to ensure it is in positive half cycle and negative half cycle. So, our modulator block will have the duty ratio which is compared with the carrier. this duty ratio $d(t)$ what we are getting from $d(t)$, depending upon the $v_s(t)$ we will generate $ds_1(t)$, $ds_2(t)$, okay using you know you can either use lookup table or you can just do the relation operation relation operation you can do and find out because we know $ds_1(t)$ is nothing but equal to $1 - d(t)$ in whenever we have v_s greater than 0 And whenever v_s is less than 0, $ds_1(t) = d(t)$. So, we can write down this $ds_1(t)$ as being equal to $1 - d(t)$, when $v_s > 0$.

and it is $d(t)$ when $v_s < 0$. Similarly, $ds_2(t) = 1 - d(t)$, is nothing but $1 - d(t)$, when $v_s < 0$, and $d(t)$ when $v_s > 0$. So, for that purpose, we can use this particular block and for generating the pwm for S3 and S4 you can take again the relation operation you can take v_s and then generate $ds_3(t)$ and $ds_4(t)$. How this will look like $ds_3(t) = 0$, for $v_s > 0$,

$ds_3(t) = 1$, for $v_s < 0$, and $ds_4(t) = 1$ when $v_s > 0$ and $ds_4(t) = 0$ when $v_s < 0$. So using these two things you can generate that and these things you can take this duty ratios let's say you've taken $ds_1(t)$ through a comparator block and having the carrier this is nothing but your carrier Now, this carrier will be at a higher frequency, nothing but the carrier frequency is nothing but f_{sw} , same as the switching frequency of S1 and S2. And that will give you PWM_{S1} .

You can also take $ds_2(t)$, or you can generate from here itself, not generate PWM_{S2} . Similarly you can take the same way comparator block $ds_2(t)$, and this you can compare and so not $ds_2(t)$, you can take $ds_2(t)$, that's not a problem this you can remove you can just write $ds_2(t)$, PWM_{S2} . Similarly you can take $ds_3(t)$ to compare it with carrier send it to PWM_{S3} and send it to compare it with the carrier to obtain PWM_{S4} . Accordingly you can design your modulator block this is nothing but the things which are there in the modulator block and that's when your all the PWMs are generated and you can send these to the gate drivers of the switches And if you take fundamentally this converter and the boost PFC converters are the same from the operation perspective.

That is when all the $G_i(s)$, and $G_v(s)$, remain the same, and accordingly, we can also select our voltage controller and current controller. Now, if you look very carefully, we have only discussed about the advantages of this converter. Now, this converter also has several disadvantages. I mean, the disadvantages are, let us discuss those disadvantages. If you look very carefully, this particular converter, in this particular converter, we have the fast switching lag, which is S1 and S2 and we have a slow switching lag, which is switches once in a line cycle, which is S3 and S4 switch, having S3 and S4 switches.

So, now if you look very carefully this particular system has this switch S1 and S2 which whose duty ratios are varying continuously in one line cycle which goes from here to here. If we try to draw the line cycle it is nothing but from here to here which is nothing but $T = 1/f_s$. In this entire line cycle if we look very carefully at during the crossings during the zero crossings whether the you know the line voltage is going from positive to negative or negative to positive.

What we will see is that during the crossings, our duty ratios of the devices S1 and S2 are changes abruptly from 0 to 1 or 1 to 0.

If we see when it is going from positive half cycle to negative half cycle, that means the voltage, the grid voltage going from positive side to the negative side, we see that our the duty ratio of S1 changes from 0 to 1. While the duty ratio of S2 changes from 1 to 0. Similarly, in case when it is going from negative to positive, that means when the voltage is going from negative side to positive side, the duty ratio of S1 changes from 1 to 0 and S2 changes from 0 to 1 abruptly. now and if we see very carefully our duty ratios let's say if we are using just the S3 and S4 switches so if we try to draw our duty ratios of let's see if we draw the duty ratio of our dS3 So, dS3 is on always during the negative half cycle.

So, we can write it is 0 in positive half cycle and it is directly going to 1 then again to 0. Here it is 0 going up to here. Similarly, if we see the duty ratio of this 4, it is 1 going to 0 and it is 0 for the entire $T/2$. period. Again, it comes back to 1 and goes to be there 1. If you look very carefully during the transition,

There is also transition of S3 and S4 whenever it is going from positive to negative or negative to positive. The duty ratios of S1 and S2 are changing from 0 to 1 or 1 to 0. At the same time my duty ratio of S3 and S4 is also changing from either 0 to 1 or 1 to 0. Now the synchronization of turning on to off or off to on of these four switches during zero crossings are the important concern you know , because in real world no two switches are are symmetrical in nature and you can never ensure that these two these timings whatever is there are synchronized and also if you look very carefully the rms current of switches in these two legs may be different that's when you also have to select different devices as well. So, when you are selecting a different device it comes with different parasitic capacitances around them and that's when they will actually have different turn on and turn off times

I mean the transition times during turn on and turn off are different and that is actually lead to the spike in the inductor currents. Now, let us see how that spike take place. Now, let us take first scenario. Now, this scenario I am talking about the point where my voltage or the grid voltage is going from the negative to positive.

That means I am talking about point A. This point, this point A. So let me write scenario 1 at point A. Now this point is nothing but, let me write slightly up so that we will have space to write down our thing. So, this is nothing but scenario 1 and if we try to see our point A where our V_s is going from negative to positive that means near to the zero crossing and if we try to draw our currents how our current look like our current So, if I draw the switching cycle average current variation, it will be looking like this. It is the same as that here, which is nothing but I can define this as $i_{s,avg}$. While my actual current

It will be of the form having the ripple over this, as we already know from our discussion. Again, I am drawing it in this fashion. It has a very small ripple. This ripple duration is very small. I have already exaggerated it just for your understanding.

So, this is my actual current, which will look like this, having the line frequency component and a ripple component riding over that. So, if we look very carefully at our scenario 1. Where we are going from, you know, the negative cycle to the positive cycle. During that time, what is happening is, if we look very carefully, my duty ratio of S2 is going from 0 to 1. So, $dS2$ goes from 0 to 1, and my $dS1$ goes from 1 to 0.

That means I have kept my entire S2 switch on while my S1 switch is completely off. So, that means S2 is on completely and S1 is off completely. During that instance, when you are at this point, my S2 goes to 1, and my S1 changes just after that point. After this point, my S1 goes from 1 to 0. So, that is what we are getting. Now, at that time, if you look very carefully, the status of S3 and S4 should be: my S3 should turn off, and my S4 should turn on.

Now if there is a delay if there is a delay in turning on S4 switch. So, what will happen during that time my S3 is on because you know you will be giving a dead time and during the dead time because you cannot turn on both the switches simultaneously. So what you will do your S3 goes from on to off so on to off it is going that means you will just remove the gate pulses so when you remove the gate pulses here S4 was already off if you look S4 was already off, so S4 was already, so when you remove the gate pulses so what has happened this diodes which are there they are you know they will depending upon the current in the circuit they will change this status from you know i mean the diode of S3 or diode of S4 is on and then only you are turning on the S4 switch so there is some time zone where your S3 has is i mean the turning on of S4 gets

delayed now during that time what is happening in the circuit is you will see the voltage across across this inductor let us see that now since the gate pulse of S3 is removed it is a dead time period but due to current the body diode of S3 is on and in that time S4 is already off As a result the entire V_o appear across switch S4 and the output capacitance of S4 is charged to this V_o voltage and then in this circuit and then in this particular circuit loop if we see where S2 is on and output capacitance of S4 is charged to V_o

The v_s value is nearly zero. So what you will get is the $v_L = V_o$. Whatever the voltage which is there on the output capacitance of S4 switch is actually coming across the inductor L. So we can write appearing across S4 switch. Now during this time what you will see is that since there is a positive voltage applied across the inductor there is a there is a positive sudden positive spike current because this voltage value will be very high generally if it is you know 400 volt so this entire 400 assume this is the 400 volt so entire 400 volt will come over here and then you will see a sudden you know high slope in the inductor current and that's when it constitute a positive spike current.

Now, in this scenario second, when assume scenario 2, again the same point at point A and v_s is going from negative to positive. So, assume if S4 is on. Now before that it was turning on and it is not turned on. So during that time what we see is that there is spike in the inductor current or you can say that there is a positive spike in inductor current. Sudden rise in the inductor current because the voltage across this become suddenly very high across inductor.

Now when the S4 is on. Whenever the S4 is on the voltage across this will no longer be V_o and that's when we have voltage across this inductor is very small or you can say that nearly zero. So when S4 is on so during that time there is no voltage across this and you will see that there is voltage V_0 with which the switch S3 capacitance get charged as S4 is already on. So what happens during that time my if S2 is on that means for longer amount of time for longer time duration My $v_L = 0$ or you can say that very small quantity.

Small quantity. And that's when it has a very small positive slope. Now, since S2 is closer to 1, that means now we are talking about we have now moved somewhere here. So, after the S4 is on, we have moved some time. So, we have seen that.

So, S2 is on for longer duration. At the same time, my S1 is on for a smaller duration because. It is because in a switching cycle if S2 is on for longer time duration the S1 can be on for remaining duration only which is very small. So during this instant when S1 is on for a smaller duration in a switching cycle the voltage across the inductor is

$$v_L = v_S - V_o$$

And since my v_S is closer to 0, what we will see is that v_L will have, this v_L is a very large negative value, very large negative quantity. And this, since we know that

$$v = L \frac{di}{dt}$$

what we see is that there is negative spike in inductor current so what we have when we are going from negative to positive there is always a delay in S4 switch whenever there is a delay in S4 switch we saw there is sudden rise in the inductor current in the positive side and whenever the S4 switch is on what we see is that there is a negative spike in the inductor current so what we will see is that when it is going from negative to positive there is a positive spike and negative spike and whenever it is and the same thing will happen in the case when it is going from positive to negative when the input voltage is going from positive to negative direction so what we see is that the inductor current if it happens to be what you want is you want your inductor current to be average variation in switching cycle is going like this and this actual current will be like this if you know if there is a large if the switching frequency is larger than the very very much larger than the line frequency then we have the inductor current. So this is your or inductor current or the input current looks like this average variation is sinusoidal but it also have a ripple current instead of that in case of totem pole PFC what you will see is that this is the ideal case ideal PFC case what we will see in case of boost PFC. What we will see is that we have average variation we have this zero crossing distortion will be there some positive spike and negative spike and this will have this waveform will be like this shape where this is nothing but at this places if you see it has nothing but called as a zero crossing distortion and this zero crossing

distortion, will actually impact the impacts THD And power factor that means if the power factor is unity it will be measuring somewhere around 0.97, 0.98, 0.99 not exactly 1. And if you look very carefully this zero crossing distortion we have discussed for going from negative to positive case.

Similarly there will also be there from positive to negative case as well. So, this every time whenever the grid voltage is going from positive to negative, we will see a zero-crossing distortion. If we assume our grid voltage is like this. This is our v_s and this will be our i_s and we have this zero-crossing distortion where the current will be crossing zero multiple times because we have positive spike as well as negative spike and that will keep on going for certain switching cycles. So, that is why we will see the positive and negative spikes for some switching cycle near to zero crossing of the line voltages, which is why this zero-crossing distortion is one of the problems in the case of totem pole PFC, especially if the output power requirement is very low at light load conditions. This distortion will be nearly equal to the peak value of the grid current, so that means this THD and power factor will be very much impacted because of that. So, that is why this zero-crossing detection needs to be addressed in the case of totem pole PFC. There are soft turn-on techniques which have been there in the literature, but one can opt to take care of this kind of zero-crossing distortion. So, in totem pole PFC, some of the advantages are: we have fewer devices, only two devices in conduction, one leg switching at a high switching frequency, and another leg switching at a low switching frequency, the same as that of the line frequency. If you have a 50 Hz AC, so 50 Hz frequency, you have reduced conduction loss, reduced switching loss, and at the same time, reduced component count. So, these are the advantages of totem pole PFC.

However, it has a disadvantage, which is having a zero-crossing distortion in the current whenever the current is crossing zero from negative to positive or positive to negative. And also, sometimes we require two kinds of switches: one for fast switching and one for slow switching. This particular thing has to be managed by the designer as well as the manufacturer when they are using this converter as an AC-to-DC converter in their EV charging system. Now, in the next lecture, we will discuss the discontinuous conduction mode of PFC converters. Thank you for patiently listening to this lecture.