CHARGING INFRASTRUCTURE

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Week-04

Lecture-18

Lec 18: Totem Pole PFC Converter

Hello everyone, welcome to lecture number 18 of this MPTL lecture series on charging infrastructure. In this lecture, we will discuss the totem pole PFC converter, which is a variant of the bridgeless PFC converter we discussed. In the last lecture, we studied some aspects of the totem pole PFC. We understood that it is, first of all, a bridgeless PFC converter where we do not have any diode bridge rectifier at its front end. Here, directly from the AC source $\left|v_s \sin sin\, \omega t\right|$, the AC is converted into the output voltage V_o, maintained at a constant value while ensuring the current drawn from the source has a sinusoidal behavior with zero phase angle between the current and the voltage, meaning unity power factor. So now we have seen the operation of that in the last lecture, where we observed that it consists of one active leg—or you can say one leg—which switches at a higher frequency f_{sw}, while the other leg, which is a diode leg, operates at the line frequency f_s. And $f_{sw} \gg f_s$, which is the condition we have been considering in the case of boost PFC converters.

Now, if we talk about its operation in the positive half cycle, let's say in one switching cycle during DTs period, S2 is on. That's when the voltage across the inductor equals the input AC voltage. So, during the DTs duration, when it is on, the current flows through the source, the inductor, the S2 switch, and then through D2 back to the source. While in the (1-D) Ts period, S2 is off and S1 is on. That's when the voltage across the inductor is $(v_s - V_o)$. If you look carefully, during both DTs and (1-D) Ts, diode D2 is always conducting. Thus, we can say that in the entire positive half-line cycle, D2 is on, and S1 and S2 switch at a high frequency. In DTs

period, S2 is on, while in (1-D) Ts period, S1 is on. This ensures the operation is similar to that of a boost PFC, where v_L equals v_S in the DTs period and $(v_s - V_o)$ in the (1-D) Ts period.

Similarly, in the negative half cycle, during the DTs period, you turn on the S1 switch. That's when D1 becomes forward-biased, and again, the voltage across the inductor equals the input v_s. And when S1 is off, you turn on S2. In the (1-D) Ts period, S2 is on. And when the S1 is off, you will turn on the S2. In (1-D) Ts period, your S2 is on.

And the current direction will be such that the current going through the D1 direction to the V_o and then coming back to the through the inductor coming back to the source again here it is the same voltage which is being I mean it is your voltage $(v_s - V_o)$ which is applying across the inductor L and that is when we do the you know volt second balance in the entire half line cycle we will get the value nothing but ,d(t) is as

$$d(t) = 1 - \frac{v_{s,pk} \sin sin\, wt}{V_0}$$

And if you see in this negative half cycle we will see that our D1 device is always on during DTs period and (1-D) Ts duration. So that's when we can say that in one switching cycle my D1 is on during negative half cycle, that's why in the entire line cycle which consists of several or which consists of so many switching cycle will also have the operation where D1 is on. So D1 is always on in the negative half cycle while D2 is always on in the positive half cycle.

In positive half cycle your D2 is always on and in negative half cycle your D1 is always on. While the S1 switch is having a duty ratio which is varying with 1-d(t) and the duty ratio of S2 is varying with d(t). In the negative half cycle, the S1 switch has duty ratio varying with d(t). While the duty ratio of S2 is varying with 1-d(t). So, if we try to draw the variation of how it looks like. So, let us draw first promising you, d(t) period. So, we know that our v_S is actually $v_S = v_{s,pk} \sin sin\, wt$.

So modulus of that we know that it goes from here to here then to here to here okay and then again let us draw one more into here to here now if we see very carefully this is nothing but my $|v_S|$ and this will have let's say Peak value, nothing but $v_{s,pk}$. And we can also say that, let us

say our V_{dc} or V_o output voltage is actually having voltage somewhat greater than your $v_{s,pk}$ to V_o voltage. So, we can draw our DTs variation of duty ratio with respect to time as so it will start from 1 when our v_S is 0 and again and it will actually vary, where this small value is nothing but $d(t) = 1 - \frac{v_{s,pk}}{V_0}$.

So, this is the $d(t)$ which is with variation with time duration T. Now let us draw the $d(t)$, let's say S1 which is also varying with time so the duty ratio of this S1 switch. So let us draw ds of this one again the maximum value is one now if you look very carefully d_{S1} is nothing but $1 - d$, so d is varying like this so we can do $1 - d$ that means it will start from 0 and it goes to the peak value and comes to 0 again if our v_s is nothing but this is positive half cycle this is negative half cycle this is again positive half cycle because here we have taken modulus, so we have drawn in the positive i mean everything in the in one side only. So, now if we see the negative half cycle in negative half cycle is my d_{S1} is nothing but equal to variation same as d. So we will now draw the d variation d_{S1} variation same as that of d it goes like this here and then again the story will repeat itself goes to 0 to 0. Here again it is at 1 and it comes to 0 and then again goes to from here to here. While this small value is nothing but $1 - \frac{v_{s,pk}}{V_0}$.

Similarly, if we try to draw the d_{S2} let us drawd_{S2} how d_{S2} will look like the duty ratio of switch S2. So the duty ratio of S2 in positive half cycle is nothing but equal to same as variation of d. So here if let's say if we define this as 1 due to maximum it can go up to 1 only.

So the duty ratio will same as d(t) goes here like this and maybe so it goes from 1 same as d(t) near to 0 and then coming back to 1. And if you see the negative half cycle my S2 is nothing but $1 - d$. So d is varying like this so it is $1 - d$, so here it is 1 so it goes to 0 here and then what we will see is that we have not exactly touching 1 but coming back to 0 and then again it follows the same as that of d(t) coming back to here like this. So it is one and then again it will have the same thing over here like this and here it will be like this so like this it is having. So, if you look very carefully, my S1 switch duty ratio is having d(t) variation in positive half cycle while the same variation as that of d in negative half cycle. Similarly, the S2 switch is having the

same variation as that of d(t) in positive line cycle while having a $1 - d$, d variation in the negative half cycle.

So if you look very carefully in every half cycle the duty ratio has to take a jump at the crossover which is one of the concern in this particular kind of converters. However, if we make sure that from the modulator block, if we make sure that somehow we vary this particular thing in this manner, we can make sure that the voltage at the output is kept constant and the current can also be maintained having the unity power factor drawn from the source. Now, if you look very carefully in this particular system, the D1 and D2, if you look very carefully, D1 is always on in negative half cycle. Where D2 is always on in positive half cycle.

So one can also instead of using this D1 and D2 diodes. Because sometimes diode have the slow recovery. And also during the conduction as well as during the unit going from reverse to forward bus. Forward bus to reverse bus they have losses which is considerable. So instead of using diodes one can use the MOSFET having the Bottle diode.

So that we can turn on the MOSFET whenever diode conducts and thus allow current to flow through its channel which give less conduction losses. The devices also have to be switched at 50 Hz or line frequency. So one can also obtain this converter something like this. This is S1, S2 and instead of D1 and D2 we can have S3 and S4 and here L,v_S is nothing but $v_s \sin sin\, wt$ and output your capacitance and resistance R_L having voltageV_o and this one is actually going to here and connected over here. So, this leg is fast switching lag switching leg having a switching frequency nothing but f_{sw} while this leg is slow switching leg having a switching frequency f_s and we can see that f_{sw} is greater thanf_s and where f_s is nothing but line frequency or you know let's say if it is a 50 Hz ac input so all 50 Hz if it is 60 Hz ac input then it is all 60 Hz and while the fsw is generally is in a 10k range 20k or 20 k Hz 30 k Hz 40 k Hz range as we discussed one can use MOSFET with body diode and then can apply required gate to source voltage to turn on the MOSFET and thus allow current to flow through the channel of the MOSFET which gives lesser conduction losses further S3 and S4 switches are switching with line frequency so switching losses is also very minimal now if you look very carefully this particular circuit what you see is that in this particular circuit you are always at any given instance of time you are just having two devices in conduction so advantage is only two devices

are in conduction at any given instance of time so that's when it helps in reducing the your conduction losses. Second you have less component count less or you can say that just four devices are needed four devices are needed and another one important expect you will see in this one is that two of the switches is having a switching frequency is having a low switching frequency low switching frequency same as that of same as that of line frequency. Now this is one of the advantage it helps in reducing the conduction losses.

So, it helps in reducing the switching losses as well. So you have switching losses in S1 and S2 switches which are switching at high switching frequency, while switching loss in S3 and S4 are minimal or nearly zero. While in the conduction losses since only two devices are in conduction at any given instance of time so conduction losses are also less. So here first point leads to less conduction losses and that's why this converter can achieve a very high efficiency, while in operation and one can also use in the fast switching leg one can also use you know modern day devices like silicon carbide and gallium nitride devices and that's when can able to achieve very high efficiencies.

Now this is the advantage of this particular totem pole PFC and that is the reason why it is been commonly used and also let us see how we can size this inductor capacitor switches. Now if we talk about inductor and capacitor it is having the value same as that of same as that of boost PFC case because you know because the operation of this is similar to that of boost PFC case. So the consideration and approximations while deriving L and C values for boost PFC case will hold true. And thus L and C values in totem pole PFC will be the same as what we obtained during boost PFC case. However, these devices if you look these devices all you know S1, S2, S3, S4 or D1, D2 they need to be sized for voltage rating decided by the output voltage V_0.

So, we can say that for S1, S1, S2, S3, S4 the voltage rating is nothing but we can take 1.4 times that of V_0, where here we have taken 40% safety margin to avoid the excessive voltage appearing on the device when it is turned off during turn off instances, so to take care that a 40 % safety margin is been given. So we understood this is our voltage rating. Now let us also see what is the current rating rms current rating i mean for this S1, S2 switches. So, let us calculate so $I_{s1,rms}$, I mean if you look very carefully S1 is on during $1 - d$ period and in positive half cycle and it is on during d(t) period in negative half cycle. So we can write for the entire time

duration of 50 Hz, which is $1/T$,we have the integral from 0 to $T/2$ in the positive half cycle, which is $1 - d(t)i^2(t)dt$, then we were in the next half cycle $T/2$ to T, our duty ratio is $d(t)$. Again this entire is in one bracket $d(t)i^2(t)dt$, will be there in the negative half cycle,

$$I_{S1,RMS} = \sqrt{\frac{1}{T}\int_0^{\frac{T}{2}} (1 - d(t)is^2(t))dt} + \sqrt{\int_{\frac{T}{2}}^{T} (d(t)is^2(t))dt}$$

and this will be taken $1/T$, where our $i_s(t)$, we assume that we are having the unity power factor,

$$i_s(t) = I_{s,pk} \sin sin\, wt\,,$$

while avoiding it is,

$$d(t) = 1 - \frac{v_{s,pk} \sin sin\, wt}{v_0}.$$

Now here if you look very carefully we can easily put this particular this thing and here if we know we already know$\omega t = 2\pi$. So from here we can easily calculate the rms this we can put this particular thing here and we can put it in any advanced computational software to obtain that $Is_{2,RMS}$ value. Similarly $Is_{2,RMS}$we can calculate again it is as,

on for 1/ T period is on in positive half cycle in positive half cycle, it was S2 was on for d(t) period, T and it is in the negative half cycle, it was on for $1 - d(t)$, and it is in the bracket.

$$I_{S1,RMS} = \sqrt{\frac{1}{T}\int_0^{\frac{T}{2}} (d(t)is^2(t))dt + \int_{\frac{T}{2}}^{T} (1 - d(t)is^2(t))dt}$$

So, if you solve this thing you can easily get what $i_{S2,rms}$ current going through the S2 switch what is the rms current going through the S1 switch voltage , we have already defined that's when you can select a appropriate S1 and S2 switch for your application. Now let us see what will be the the rms current through the S3 and S4 switch. So if i try to write $i_{S3,rms}$, which is nothing but 1 by for the entire line cycle if we talk S3 if we just talk about S3 switch this S3

switch is on for in negative half cycle. So it is only from T / 2T period $i_s^2 dt$, only this much will be the rms which was not the case over here where we have in the both the cycles where S1 and S2 where they are in both the cycles different duty ratios were there here there is no duty ratio because no duty ratio term because this S3 switch is on for the entire negative half cycle, that's when we were just taking the duty equal to 1,

$$I_{S3,RMS} = \sqrt{\frac{1}{T}\int_{\frac{T}{2}}^{T} (is^2(t))dt} = \frac{I_{s,pk}}{2}$$

While if you take $i_{S4,rms}$ is nothing but 1 / T going from 0 to T /2, $i_s^2 dt$, and if we assume that is t is nothing but $i_{s,pk} \sin sin\, wt$, then we will get this one, nothing but $i_{s,pk}/2$

$$I_{S4,RMS} = \sqrt{\frac{1}{T}\int_{0}^{T/2} (is^2(t))dt} = \frac{I_{s,pk}}{2}$$

Here we will take. Let also is peak by, so accordingly, we can also select our S3 and S4 switch. And these two will have different current ratings. So accordingly, one can choose two devices or one can choose a single device to maintain uniform inventory in the system. Now, if we talk about it, we have understood how we can size these components. We also see how we can size these switches. Now, another important thing which we have to do is how we can do the closed-loop control where we ensure that output voltages are maintained at a constant output voltage V_0, and along with that, the unity power factor current can be drawn from the source. So, in this, we will follow the same principle that we have followed in the case of the boost PFC case, and we can again design our closed-loop control for obtaining those control objectives. So, thank you. We will meet in the next lecture and we will discuss that. Thank you.