CHARGING INFRASTRUCTURE

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Lecture-17

Lec 17: Bridgeless PFC Converter

Hello everyone welcome to the lecture number 17 of the NPTEL lecture series on charging infrastructure and today we will see another variant of PFC converter which is a bridgeless PFC converter. Before starting the discussion let us discuss what we have seen up till now and what we infer from that particular discussions so in this we have seen the boost pfc converter what we have is where we have full bridge diode rectifier and followed by a boost dc dc converter boost dc-dc converter boost converter we have and before that we have a full bridge diode rectifier. Now in this we have seen that this vd what we are getting is nothing but the $\left|v_{s,pk} \sin sin\ \omega t\right|$ and then we varied our duty ratio of S1 and S2 in such a manner that on an average sense we are drawing the unity power factor current from the input source and at the same time the output voltage is kept constant, even though the v_d is having rectified voltage before having a voltage looks something like this. So, where we have seen that our duty ratio d(t) of t with respect to time actually varies from here to here and then in this manner as a result of which we will be in a position to obtain a voltage V_0 assume this is your V_0 voltage and this is nothing but your $v_{s,pk}$ voltage we have. So that is the scenario we are we have seen so where if we vary our duty ratio in this way we will be in a position to make sure our output voltage is kept constant at the same time since the duty ratio is varied we are in a position to to actually apply a v_{conv} voltage and that v_{conv} voltage is such that the current drawn from the v_d source will also be following the same pattern and without having any phase difference as a result of which the current drawn from the source will be the unity power factor current. Thus, we can do two things we can able to maintain the output voltage along with that we will be in a position to have the unity power factor current drawn from the source. However in this case we have seen that our current which has been drawn from these input source i_s current will have a average variation of a sinusoidal manner and having a zero having the zero phase shift with respect to the AC voltage source however inductor current will have ripple over that and that ripple and the average variation of that is varied in such a manner that we have the sinusoidal current drawn from the the average variation will be such that the average current will have or the is is actually the green colour waveform however the average variation is having the sinusoidal component so this particular i_s current which looks something like this something like this sort will have the frequency component of line frequency fs and then after that it has the switching frequency component which is fsw and fsw we have kept in switching frequency we have kept very very much greater than fs which is somewhere greater than 20 kHz or 30 kHz 40 kHz where our line frequency is just 50 Hz so we can say the component the ripple component is very small as compared to the line frequency component So that is what we have understood. We have also seen different ratings of these devices, inductor, capacitor. This switches S1 and S2. We have seen the voltage and current ratings.

We have seen the value of L, the value of C. We have also seen the presence of second-line harmonic voltage ripple on the capacitor C. So, the output voltage has the DC component over which that second-line harmonic voltage ripple will be present. And the C will be designed in such a manner that the second-line frequency component voltage ripple is as small as possible within the permissible limit. So, this is what we have discussed in this section, and then we have also seen the closed-loop control, dual closed-loop control, where the control objectives were to maintain the output voltage at the desired value, obviously greater than the maximum voltage at the input, that is, greater than vs,pk. Along with that, we are making sure the current, the average variation of current drawn from the source, will also be sinusoidal and have zero phase difference compared to the line voltage, thus ensuring we have the unity power factor current drawn from the source.

So, those control objectives we have seen, and we have also seen what the plant model is to derive the controller parameters. We have also seen, and briefly understood, what the criteria are for designing the controllers. And we have seen the constant frequency control, where we are just changing the duty ratio. One can also use hysteresis control, where they can vary the current ripple within a fixed band, and that band could be constant or variable. So, all those things we have gone through in our previous discussion.

Now, let us discuss another variation of this boost PFC converter, which is the bridgeless converter. Now, here, if you look very carefully, the boost PFC converter has the input full-bridge rectifier. If we see very carefully, let us say in the positive half-cycle, we have diode D1 in conduction. Let us say during the DTs period, our switch S1 is under conduction, and then our diode D4 is under conduction. While in positive half cycle, in (1-D)Ts period, we have D1 diode is in conduction. We have switch S2 in conduction, and then we have diode D4 in conduction in the positive half-cycle.

This is during DTs period, during (1-D)Ts period. However, in negative half cycle that means when the Vs voltage I mean the AC input voltage Vs voltage is in negative half cycle or having a negative value. During that point what we have seen is that it is our D2 is in conduction then again S1 in D again during negative half cycle during DTs period our S1 is in under conduction and then our D3 is under conduction. While in (1-D)Ts period, it is D2, S2 and D3 is under conduction. So, in any given instance of time, we see that there are 3 switches or 3 semiconductor devices which are in conduction.

Now, that leads to higher conduction losses. And at the same time, we see that our number of component count if we see is also high because we have 4 diodes, 2 switches, inductor, capacitor are being used. So, there are two you know weak point of this converter or disadvantage of this converter which is higher component count and along with this we have three devices in conduction at any given instance of time. So, thus we have pretty good conduction losses also associated with this converter.

So, now let us see how the bridgeless PFC will solve these two particular problems. so if you look here in this bridgeless PFC converter what we have is since in case of boost PFC case we have the diode bridge rectifier at the front stage and then followed by DC-DC boost stage. In this case we do not have the front stage diode bridge rectifier here what we have is we have the we have actually four devices and these four devices are arranged in a manner where we have D1 and D2 which are the diodes while S1 and S2 are the active switches you know active switches with the diode connected across it mostly it is the MOSFETs which are being used along with their body diode which are being used so we represent this you know this switch accordingly. So, now in this case, we have four devices and where two diodes are there and two, you can say a MOSFET with a body diode are there. And also along with that, we have L and C which are there and we have, you know, $\left| v_{s,pk} \sin sin\ \omega t \right|$ which has been there.

And this is actually being, you know, being used, you know, in positive half cycle and I mean it has been operated in positive and negative half cycle. Now, let us see how in positive and negative half cycle it works. In positive half cycle, what we do is we only switch the switch S1. We only give the to switch S1. Now, when we turn on this switch S1, the thing is the current will start flowing from here and it will go through the, let us say if it is a MOSFET, then it will go through its channel between drain to source and then from there on the other side,It will find the pathway through the podial diode of the switch S2.

So now the MOSFET turns on the current is flowing through the inductor through switch S1 and then the diode of switch S2. And then it will go back to the source, you know, which is just nothing but a Vs(t), which is as we define over a $v_{s,pk} \sin sin\ \omega t$. Now, this if you see, if you apply the KVL, what we will get is we have VL equal to Vs which is been applied across the you know VL is the voltage across the inductor the voltage across the inductor is nothing but equal to Vs(t)

$$v_L = v_s = v_s(t)$$

you know Vs(t) you can say or you know alternatively we are also writing just Vs, that is the case in the DTs duration where we are turning on our S1 switch. So in the DTs duration where D is the duty ratio and the DTs is the period when the switch S1 is on in in you know in the switching cycle sense here we have taken Ts where Ts corresponds to 1/fsw and we know that fsw is very very much greater than our fs where fs is the line frequency. As we have already taken into consideration.

So, in you know in switching period sense in switching cycle sense this S1 it turns on for DTs period and that is when the current is flowing in this manner. Then in (1-D)Ts period when the switch S1 is open when the moment the switch S1 is open the inductor current which is there which is developed has to find a pathway as a result of which this D1 gets forward by us and the current will start flowing through this through the load and then it comes back through the diode of S2 switch or you can say the body diode of the MOSFET and comes back to the source. Now, as a result of which, what we have is, we have our, if we try to write down the KVL in this loop, what we have is the voltage across the inductor v_L is

$$v_L = v_s - v_o = v_s(t) - v_o$$

And if you look very carefully in the positive half cycle, we are not giving any any gate we are not giving any gate pulses to S2 switch we are not turning on S2 switch I mean if the MOSFET is there we are not turning on its channel only the diode across the device is conducting in the S2 which is connected across the S2 switch but S2 switch is not being turned on. So, the S2 switch will not be in operation in the positive half cycle and also if you see the D2 will also be not in operation in the positive half cycle in the entire positive half cycle. In the negative half cycle, during the DTs period or during the DTs duration, I mean, as in case of positive half cycle during the DTs period, we have given gate pulses or we have given gate signal to S1 switch. In negative half cycle, what we do is, instead of giving gate signal to S1 switch, we are giving gate signal to the S2 switch as a result of which this S2 switch turns on and the current will start flowing through this and returns and find its pathway backwards to the source via this the body diode of the MOSFET and if you wanted to have the better conduction performance or you can say less conduction loss.

So what you can do is you can also turn on this channel, so that the current will go through the channel. Now in this case , so in DTs period the current will going through the S2 switch and it will return back to the source. Now, in this case, when we see our, if we take the inductor, voltage across inductor polarity in a reverse direction as our current is going in a reverse direction across the L. So, what we can write here is that our minus VL, the voltage across inductor is minus v_L minus, you know, Vs. I mean, if we say Vs(t), we write.

And, you know, in (1 – D)Ts period, when, you know, the gate signal sent to S2 switch is opened, when it is been opened, the current through the inductor will force the D2 or the D2 will get turned on, and as a result of this, the current will go through the load and then it will return. It will find this pathway through the body diode of the MOSFET and then find path back to the, source. So, here we can write you know if we do the KVL again the current is in the opposite direction. So, polarity of the voltage across the inductor will be in a reverse direction.

So, when we write what we will get is we will get minus VL equals V0 minus Vs of T, or we can then write our VL equals our VL is then equal to Vs minus V naught.

$$-\nu_L = \nu_o - \nu_s(t)$$

$$\nu_L = \nu_s(t) - v_o$$

So, if we see, if we write our expressions, in the positive half cycle, we have during DTs duration, we have VL equal to Vs,

$$\nu_L = \nu_s$$

and during 1-D(Ts) duration, our VL equals Vs minus Vo.

$$\nu_L = \nu_s - V_o$$

Again, this Vs is Vs(t), the same thing.

In the negative half cycle. During the DTs period, if you see, it was minus VL minus Vs(t), Vs (t) minus VL minus Vs(t). So, we can write VL is directly equal to Vs,

$$\nu_L = \nu_s$$

and in the 1-D(Ts) period, VL is nothing but, if you see, Vs(t) minus V0.

$$\nu_L = \nu_s(t) - V_o$$

That is when we can write the voltage across the inductor during DTs duration. We can write it is nothing but |Vs| because only the magnitude has been there and in (1-D)Ts period. the ν_L voltage across the inductor is as:

$$\nu_L = \nu_s - V_o$$

And it is similar to that of, if you look very carefully, our boost PFC case. And thus, when we do the volt-second balance over the half-line cycle, we will get, I mean, in the same manner as we have done during the boost PFC case, and then take the approximation, what we will get is our duty ratio is varied the same as that of the boost PFC.

So, our duty ratio will vary accordingly. So, our duty ratio will vary the same as that of the boost PFC case, which is ,

$$d(t) = 1 - \frac{v_{s,pk} \sin sin\, wt}{v_0}$$

Now, this is the duty ratio, duty which has to vary over the entire half-line cycle. So, we can then write, if we see in the positive half cycle, only the S1 switch is getting that duty ratio signal. I mean, only the S1 switch is turned on and turned off during the switching period time in the, I mean, for the D(Ts) duration, while it is off for (1-D)Ts duration.

So, we can then write our duty ratio of S1 switch is equals to d(t) when our Vs is greater than 0 and in the if you see in the negative half cycle the S1 switch is not at all being given the signal gate signal or it is completely off. So, we can and only the current is going only through the diode or diode which is connected across the device so it is nothing but the ds1(t) is nothing but equal to equal to 0 or Vs less than 0.

$$d_{s_1}(t) = d(t), v_S > 0$$

$$= 0, \quad v_S < 0$$

Similarly, we can also write for ds or we can also write for switch S2 the duty ratio will be in positive half cycle S2 is not will not be turned on and off during D(Ts) and (1 -D)Ts period it is completely off. So we can then write duty ratio is nothing but 0 or Vs greater than zero and in the negative half cycle is the S2 switch which turns on during the gts period and turns off during the (1 -D)Ts period so the duty ratio of dS2 switch is nothing but d(t).

$$d_{s_2}(t) = 0, v_S > 0$$

$$= d(t) \quad v_S < 0$$

And if you see in any , I mean in any given instance of time what we see is that and if you see in any given instance of time the two of your devices are in conduction you know in this period also it's the S1 switch and the diode which is connected across the S2 switch or you can say the body diode if we if MOSFET is used in (1 -D)Ts period also it is the diode D1 and the diode which is connected to S2 switch in negative half cycle also if you see in D(Ts) period it's the S2 switch and the diode which is connected across the device S1 and that means the body diode, the MOSFET is used, and during the (1 -D)Ts period, the D2 and body diode are connected across the device S1 diode. So, in so we can say that at any given instance two devices are in conduction.

So, let us see how our d(t) varies. So, if we try to draw if my Vs is like this as if this is Vs, which has $V_{s,pk}$ and this is T and we have our Vo voltage let's say greater than $V_{s,pk}$ this is our Vo voltage. So, our duty ratio will be of the form goes from here to here not going to zero because we have assumed that Vo is greater than this 1. So, this at this point the peak the minimum value so this is nothing but a d(t) and here we have close to 1 during at that point then close to 0 during this point where this is nothing but $1 - \frac{|v_{s,pk}|}{V_o}$ this is the minimum at minimum value. So, this is what you will get and near to the closer to 0 our duty is nothing but 1, And then, so it is near to 1 because our Vs is nothing but equal to 0. So, we have 1 going from and going near to 0, not exactly 0.

And if we take V_o equal to $V_{s,pk}$, then this is 0. Otherwise, it is very close to 0. This and this value is same. So, this is a duty ratio variation, which is the same as that of the case of boost PFC converter case. However, there is no doubt build rectifier and if you look very carefully, so in both the DTs period and (1-D)Ts period, only two devices are in conduction.

So, we can see that at any instance, any time instance, only two devices are in conduction. Thus, having a lower conduction loss as compared to that of the boost PFC case. And one more thing you will see here, we have only 1, 2, 3, 4, four devices, only four devices need to be used. As compared to six devices in case of boost PFC with the full bridge diode rectifier now the disadvantage with this is if you see a one disadvantage in this particular kind of system is this diode D1 and D2 which are there these are switching at switching frequency $f_{s\omega}$ which was not the case in case of boost psc where we have the diodes at the first stage because there the diodes are switching at the line frequency here the diodes need to switch at higher switching frequency and which is at fsw so disadvantage is diodes need to switch at $f_{s\omega}$ that means it turns on and turn off at higher switching frequency and here $f_{s\omega}$ is greater than very very much greater than f_s line frequency. While in case of boost PFC where we have the diode bridge rectifier at the front stage our diodes were switching at or our diodes are forward bias and reverse bias only one of this cycle it is on another half cycle it is off. So, only once it is switched in one line cycle. However, here it has to switch or it has to go from off to on or on to off at every switching period or at every switching frequency period and that switching frequency is very much greater than f_s. So, thus fast recovery diode has to be used. Need to be used. And this also lead to higher losses associated with diode. This is the disadvantage of this particular converter.

However, if you see the L value, C value, it is the same as that of what we have calculated during the boost PFC case, but here the diode whatever are there has to be very you know fast reactive one or very fast recovery diodes need to be used and here the reverse recovery losses are enormously very high since the diodes are switching at or are getting are becoming off and on in every switching cycle and this switching cycle is very very smaller as compared to that of the line cycle or line cycle period so that's why this lot of losses i mean huge losses associated with the diodes are there which is one of the disadvantage.

So, this is the problem with this bridgeless PFC. Now, this bridgeless PFC since this diodes are switching at a frequency which is very much larger than the line frequency or you can say that the diode need to be very fast recovery that we can avoid by using another kind of derived topology of bridgeless PFC you can say is nothing but called as a totem pole PFC. It is one of the commonly used pfc topologies or you can say bridgeless PFC topologies which are being used the reason being we will see here. So in this if you look very carefully we have again four devices that means two switches and two diodes which are rearranged in a fashion such that we have one leg as active half bridge and one leg as diode based half bridge. Here S1 and S2 switches are mostly realized using MOSFETs and the diodes shown over here are the body diodes of MOSFET. It is because, whenever the body diode is in conduction one can turn on the MOSFET by applying required gate to source voltage and thus allow the current to flow through the channel which gives very less conduction losses. In this case here we assume when MOSFET turns on the voltage drop across the channel is very less which will not forward bias the body diode. One can also use IGBT to realize S1 and S2 switches but in that case one has to connect freewheeling diode across the switch so that when the current is in negative direction it can flow through the freewheeling diode. However, in this lecture we will only consider S1 and S2 as MOSFETs. Let us see the functionality of that, in this, in the positive half cycle, again in the positive half cycle, in one of the switching period when the, let us say when the duty ratio are the constant value D, capital D. So, during that time, what happens is that in DTs period, my S2 is on.

Now, the moment the S2 is on, this here you are having $\left|v_{s,pk} \sin sin\ \omega t\right|$ coming over here the moment this thing is there in a positive half cycle. This is positive where your v_s is greater than zero here it is v_s so at that point you are having positive voltage applied over here across the inductor this S2 is on so the current will start going like this and through the D2, D2 will get forward bias and since this get forward bias if this get forward bias then automatically this entire V_O will be appearing across D1 and that's when D1 is reversed bias and as a result of which you will see that across the inductor the voltage applied is nothing but v_L is nothing but v_s. In (1-D)Ts period the switch S2 is turned off as a result the inductor current will find its path through the body diode of S1 and thus we can turn on the S1 switch that means S1 switch is on during (1-D)Ts period. Now the moment to turn on this S1 switch what happens is that,the current will start instead of going through the S2 switch, it is going through the S1 switch. And that's when it goes to the S1 switch through the load. It comes back and again D2 gets forward bias and then it comes back into the source, which is nothing but $v_{s,pk} \sin sin\ \omega t$. So here, if you look very carefully in both the DTs period and (1-D)Ts period, D2 is on. D2 is on in both the period. both in DTs period and (1-D)Ts period.

So, thus the D2 is on in the entire switching period and it is one of the switching period. So, in all the switching period in the positive half cycle your D2 is on. That means it is working like a you know in case of full bridge rectifier where we have the diodes are forward biased in one half cycle and allows current to pass through it. And it is off in the rest of the half cycle. So, thus here also it is the same thing in positive half cycle D2 is on. While in the negative half cycle. In the negative half cycle same thing. In one of the DTs period in the negative half cycle. The S1 is on in DTs period.

Here S1 is on. If you see S1 is on. During that time, since it is a negative half cycle, the current will start through this and from here, from the source in this direction and since in this one, this current will actually forward by this D1 and as a result of this D1 is on and then you have the same thing which is nothing but the VL which will have the same Vs input voltage applied across it. In (1-D)Ts period, the S1 switch is turned off. As a result, the inductor current will find its path through body diode of S2 and thus we can turn on the S2 switch that means S2 switch turns on during (1-D)Ts period in negative half cycle.

And as a result of which you will see that that D1 because of the current direction D1 is forward bias and thus the current goes through the Vo voltage and comes back to L again. Here also the voltage across inductor is

$$v_L = v_S - V_O$$

So what we see is that in the DTs period the v_L the voltage across inductor is nothing but Vs. In the (1-D)Ts period let us say in the positive half cycle my v_L is nothing but Vs. Vs minus Vo and that we do the same thing. It is the same case as that of the boost PFC case. What we get is

$$d(t) = 1 - \frac{|v_{s,pk}|}{V_o}.$$

It is the same duty ratio we get. However, we see that in positive half cycle S2 is switched with this duty cycle. and S1 is switched with 1 minus this duty cycle while in negative half cycle is the S1 is switched with this duty cycle value and S2 is switched with 1 minus this duty cycle value. So, here it's in the positive half cycle and in negative half cycle it's the duty ratio with which S1 and S2 is on gets changed at in every half cycle.

And along with this, if you look very carefully in the positive half cycle, only D2 is on. In the negative half cycle, always D1 is on. Why always D1 is on? Because during d(ts) period and 1 minus d(ts) period in the negative half cycle, always my D1 is in conduction, I mean is forward bias and is on. And that is when our D1 is always on in negative half cycle.

So, what we infer from this is, in this particular totem pole PFC because we are giving S1 and S2 duty ratio in such a manner that we make sure that this only this S1 and S2 switches with high switching frequency which is $f_{s\omega}$ while D1 and D2 are switches with line frequency which is f_s and we know that we have $f_{s\omega}$ is very very much greater than f_s and so we can say that . The operation is such that it has two legs where one of the legs are fast switching leg while other one is slow switching or you can say line line frequency switching lag okay you can say that and this is nothing but one of the advantage with this totem pole PFC converter that S1 and S2 are switching at a faster switching frequency, while D1 and D2 are forward and reverse but in the line frequency period. And thus, we do not need a fast recovery D1 and D2 diode.

It can be done with the slow recovery diode itself. That is one of the advantages with this. And in any given instance, only two devices are coming in conduction. And if we look very carefully, in positive half cycle, the duty ratio of S1 we can say that it is 1-d(t) while duty ratio of S2 is nothing but d and in negative half cycle

the ds1 is nothing but duty ratio of S1 switch is nothing but d(t) while duty ratio of S2 switch is nothing but $1 - d(t)$, and we know that our $d(t)$, is

$$d(t) = 1 - \frac{\left|v_{s,pk} Sin\omega t\right|}{V_o}.$$

V_o that we have already derived in case of boost PFC and we can say that. During this period in positive half cycle only D1 is on. I mean you can say that out of D1 and D2. Here always D1 is on. Always D1 is on.

While in negative half sorry always D2 is on. While in negative half cycle always D1 is on. So, this is the thing we got from our understanding of totem pole PFC that in positive half cycle my S2 is switching with d(t). I mean during DTs period, S2 is on and (1-d)Ts period S1 is on. While in negative half cycle my S1 is on with d(t) and S2 is on with (1-d)Ts, while d2 is on for the entire positive line cycle or half cycle and D1 is on for the entire negative half cycle now we will discuss further on this in the next class or in the next lecture thank you for patiently listening to this lecture