Course name- Analog VLSI Design (108104193)
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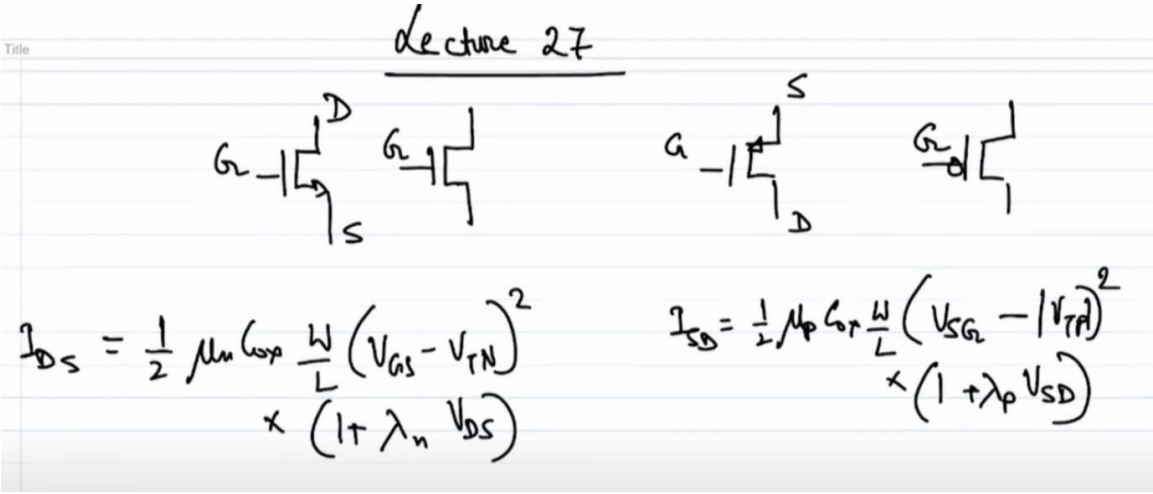
Week- 9
Lecture- 27

Welcome back and this is lecture 27. So, in the previous lecture we were looking into how to use PMOS in place of a in place of a resistor and we came up with an architecture where it seemed like we should be able to we should be able to replace a resistor with a PMOS transistor and get high gain in a common source amplifier right. So, before proceeding with the same thing let us have a quick recap on the differences between an NMOS transistor and the PMOS transistors characteristics right. So, that will be useful in the long run. So, this is a PMOS transistor, this is this is NMOS transistor and this is a PMOS transistor. So, the arrow always points indicates the source terminal.

So, this is drain, this is source, this is gate, this is source, this is gate, this is drain. Very often you will see that another symbol is used to refer to the PMOS and the NMOS and that symbol is the following without the arrow. This is under the understanding that you we I mean we know that this is a gate, but we do not know which side is the which side is the drain or the source right. So, this happens quite often if the voltages of the terminals of drain and source can clip right.

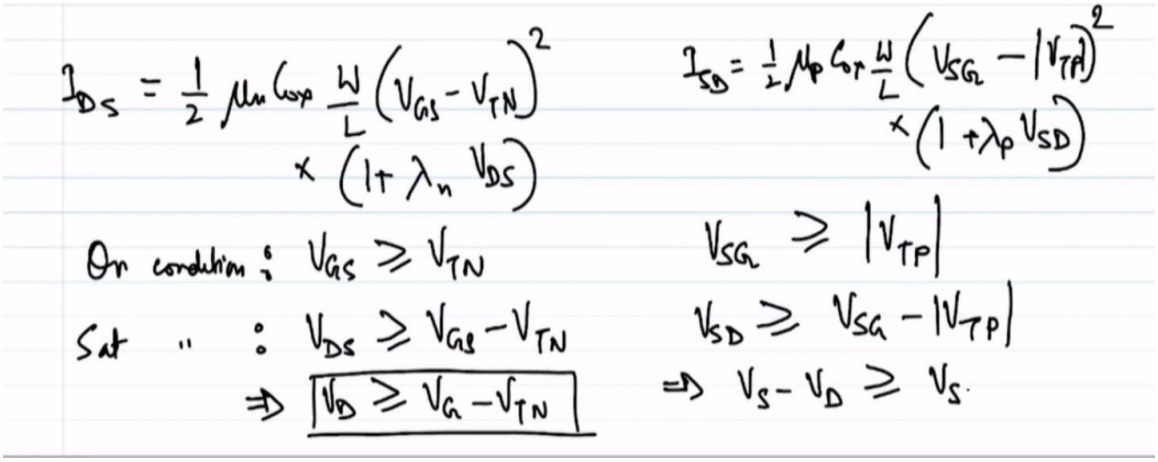


One side can be higher, other side can be lower. We really do not know which is drain and source it completely depends on what the application is or what the which side is the higher voltage right or which side is a lower voltage. And sometimes you will see that that symbols are expressed without the arrow with the understanding that as an user or as a designer we know which side will be the source or the drain. Similarly, in case of a PMOS the similar symbol is the following we have a bubble at the gate right. We have a bubble at the gate

and we have terminals without the arrow again with the understanding that if we know which is the higher terminal we will ascribe that terminal to source and the lower terminal lower voltage terminal will be ascribed as the drain right.

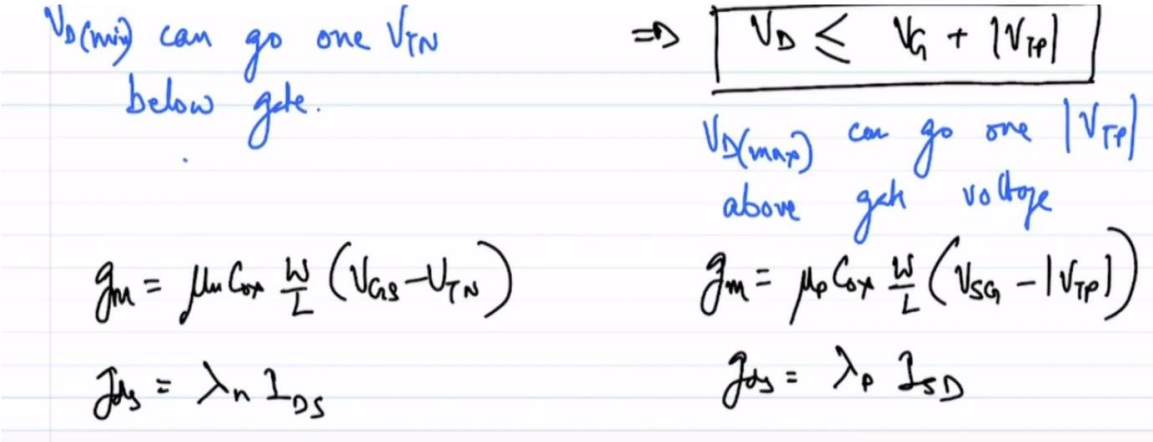
So, since we are dealing with PMOS and NMOS's I thought you should be you should be you should be aware of this of the symbolic differences also ok. So, quick recap in saturation IDS for NMOS is half mu n Cox W over L Cgs minus Vtn whole square. In case of a PMOS Isd is equal to half mu p C ox W over L Vsg minus mod of Vtp whole square. If I have to include channel length modulation then this becomes 1 plus lambda n VTh then this becomes into 1 plus lambda Vsd right ok. So, what is the expression what is the condition for what is the saturation region condition? The saturation region condition for or rather what is the on condition in case of a NMOS on condition is.

So, let me say this is the on condition on condition for the NMOS is Vgs has to be greater than equal to threshold voltage Vtn in this case because we have been expressing it like that ok. So, what is the on condition in case of a PMOS on condition is Vsg should be greater than equal to modulus of Vtp right. Again note that in most cases Vtp is a negative quantity, but in that case we refer to Vtp with respect to Vgs, but since we are referring with respect to Vsg we are more interested in the mod of Vtp because dealing with negative quantities can be sometimes lead to some confusion in terms of which side the current directions are right ok. So, what is the condition on saturation region? Saturation region condition is Vds should be greater than Vgs minus threshold voltage which implies the drain voltage should be greater than the grid voltage minus threshold voltage. This is the condition that we were using throughout the course.



So, what is the corresponding condition in case of a PMOS? The corresponding condition is if we if we if we simply say that everything is reversed right source becomes drain, drain becomes source and so on. So, if we just use that if we just use that that understanding we should be we should write it as V s d should be greater than equal to V yeah Vsd should be equal to Vsg minus mod of Vtp VT Vtp ok, which essentially means that Vs minus Vd should be greater than V s minus V g minus mod of Vtp right, which means this goes off

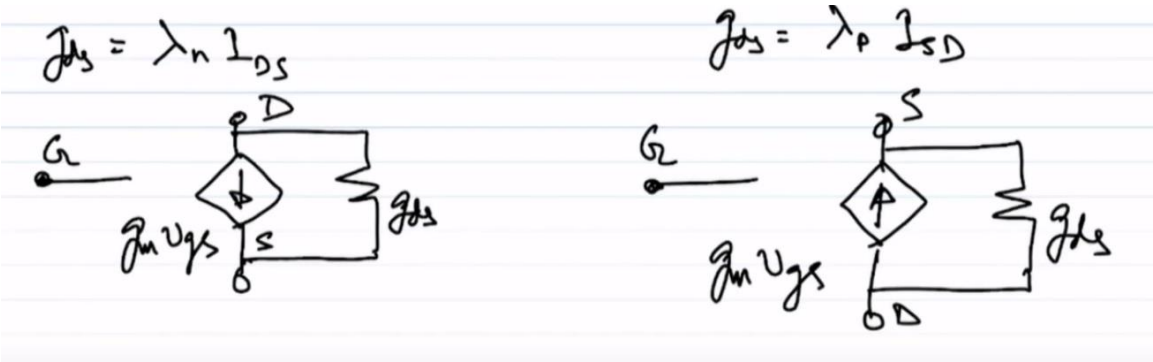
which means Vd should be less than equal to Vg plus mod of Vd right. So, this becomes a saturation region condition. In plain English in plain English the the the saturation region condition for an NMOS is is Vd can go 1 threshold voltage below gate right can that. So, this is a minima condition of so, this is a this is a Vd minimum can go 1 threshold voltage below gate in case of a PMOS this will be Vd has to be less than something which means this is the condition of Vd maximum right.



So, in case of this this is Vdmax can go 1 threshold voltage above the gate voltage ok. Then what else what are the small signal parameters? The small signal parameters in case of NMOS is gm is equal to I mean you know mu n Cox W over L Vgs minus Vtn in this case in the case of PMOS it will be gm is equal to mu p Cox W over L Vsg minus mod of Vtp right. Similarly, you can write in terms of similarly you can write in terms of current where under root current term will come similarly gds is lambda n Ids here gds will be lambda p Isd because the current of Isd is positive ok. What is the final thing that we should see? The final thing that we should see is a small signal model. The small signal model we we we discussed that both the small signal models are identical, but that we we choose to draw it in a slightly different manner because because ultimately we know that the drain in case of a NMOS is on top and the drain in case of a PMOS is generally on the bottom because drain is at a lower potential right in in a quiescent condition right not necessarily in the incremental condition.

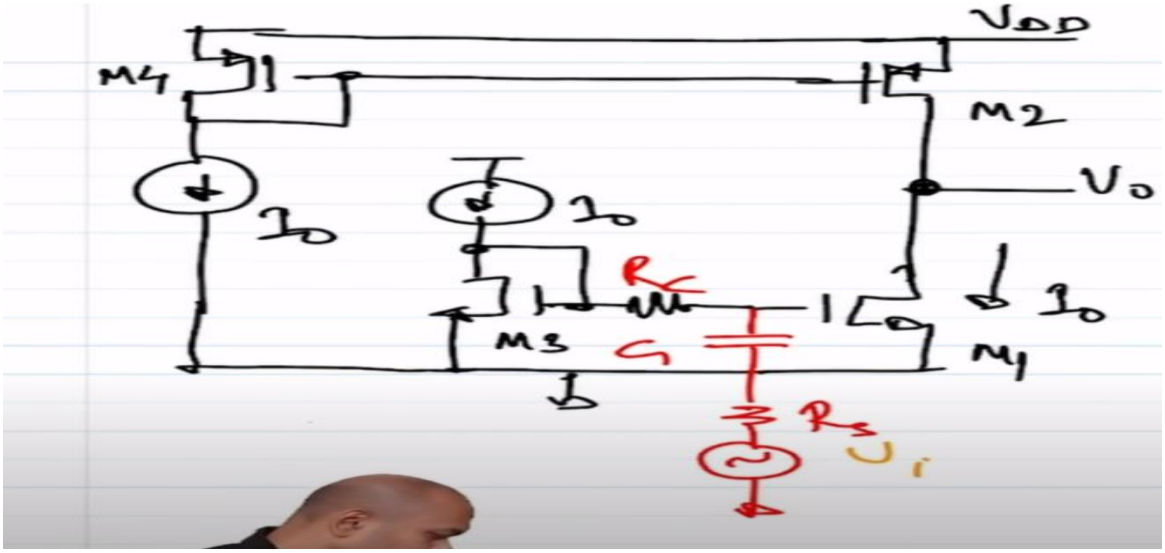
So, this is gate, this is drain, this is source and this is gm times Vgs and this is g ds in case of a NMOS. So, in case of a PMOS we have again the gate remains gate, but we call the top terminal source and the bottom terminal drain this is gds. Again this current we will call at g as gm Vgs, but now since the incrementally both are same the current has to go from drain to source just like in the circuit in the left. So, the arrow points upwards right ok. So, that is as far as we need to know about about the PMOS equivalent with respect to NMOS.

And now we will treat it as almost the in terms of the incremental equivalent it is it is basically the brother of NMOS right right with one critical difference the only critical



difference is the lower terminal the lower voltage terminal is a drain voltage ok fine. And obviously, there is another critical difference and that is the on condition here is Vsg has to be greater than Vtp right. So, these two if you keep these two in mind then we are good to go ok. So, what was it that we what was what was the circuit that we were discussing when we stopped in the previous lecture the circuit we were discussing was we were having a common source amplifier right and this was biased using ok.

So, hold on. So, we had a common source amplifier this was biased using a current mirror right and because this was biased using a current mirror and we wanted to feed the input. So, we had to uncouple we had to ensure that the input is AC coupled. So, this is R c this is the Rs this is the Rc this is C infinity or we can call this C1 or C infinity it really does not matter ok. So, this we have already done long time back in this course the only difference here was instead of putting this RL here we would have like to put a PMOS transistor right. So, this was Vdd, but this PMOS transistor needed to be biased for the same current Io right for the same current Io and how did we bias we saw that that we basically will be using the biasing scheme of this structure to bias the NMOS bias the PMOS for a current of Io.



So, we use the same current mirror based bias and we put Io here right. So, let us name

them let us say this is called this M1, this is M2, let us call this M3, M4 ok and this becomes this becomes our this becomes our Vo ok. So, again note that we this does not really ensure that both M1 and M2 is in saturation, if we assume that they are in saturation then this combination of this combination of M1 and M2 is is essentially our common source amplifier right. So, I had asked you to sketch the small signal equivalent of this and figure out what is what will be Vo over Vi, I hope you have done that let me quickly run you through what needs to be done right. So, all we need to do is I mean replace all the transistors with their incremental equivalent.

So, let us do that let us start with M1, if I neglect the gds then life becomes slightly easier and we can let us do that for the time being and then we linked out introduce gds later. So, M1 has a gate right and this is M3 is a grounded right, what is that M3 is driven by current source the current source opens up, but the gate of the M3 is connected to the drain of M3. So, incrementally this becomes that so this is gate, this is drain right. Now, what happens to and what can you replace this, what is the impedance looking in into this terminal, the gate then drain connected terminal we have done this before the impedance looking in is 1 over gm right. So, we can replace this entire structure with 1 over gm, 1 over gm to ground right.

So, you have an Rc here ok, then this capacitor this is Rs this is Vi ok and if we replace if we size the capacitor in such a way that it is like short circuit at the signal frequency and if we size Rc in such a way that Rc is much much greater than Rs right. So, if C1 tends to infinity and Rc plus 1 over gm is much much greater than Rs and what can we do we can we basically then we can infer that this guy does not load Vi. So, that contraption gives you effectively infinite impedance. So, and C is a short circuit which means this voltage here is approximately Vi, if that is Vi I can remove all this stuff right, I can remove all this stuff and I can assume that this voltage is a gate voltage of M1 is Vi. So, this current becomes gm1 times Vi ok.

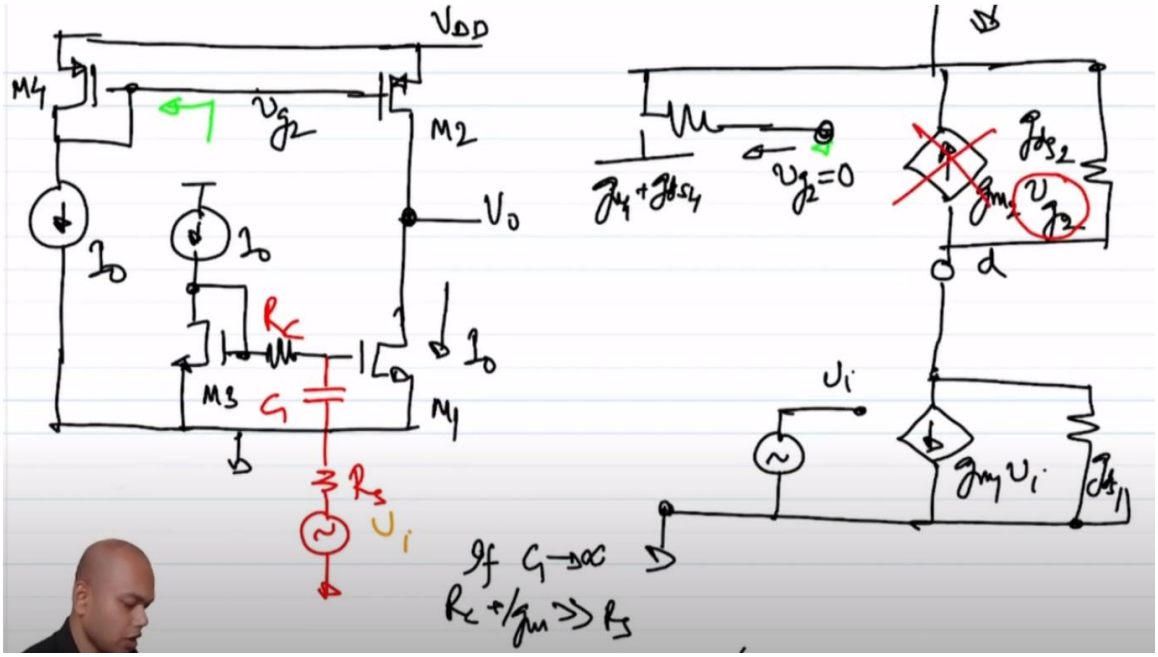
So, M3 basically goes out of the picture. So, let us go on the top and concentrate on what is going to happen with M2. So, what is going to happen with M2? So, what will you do? We will replace the incremental equivalent of a PMOS, what is the incremental equivalent of a PMOS right, incremental equivalent structure of a PMOS is this guy ok. So, we will basically replace that.

So, let us do that. So, this is the drain, this is the source, this is g m V g s moving upwards right and this is the gate and this drain and this drain are connected together and let me mark it as gm2 right gm2 Vgs ok. Instead of saying Vgs all the time let me call this Vg2. So, this becomes so, this terminal is Vg2. So, this is gm2 times Vg2 minus Vs, what is V s? Incrementally what is Vs? S is connected to Vd d, Vdd is short circuit. So, incrementally

source is shorted correct.

So, this becomes gm2 times Vg2 right, we do not have to bother about, we do not have to bother about the source terminal right. So, this is like the bottom terminal I mean this is like the case with M1 also right ok fine. What is happening with M4? So, this is anyway shorted right. So, same thing let us replace our stuff with. So, this is we have a current source here.

So, current source opens up, this is the drain voltage, the drain and the gate are connected together, the drain and the gate are connected together and this is gm3 or gm4, gm4 Vg2 right gm Vgs or gm4 Vg2 correct ok great. So, can we simplify this contraption, can we simplify this contraption? What is the impedance looking in, what is the impedance looking into gate of this of this guy, what is the impedance looking in gate of M4? Because the gate and the drain are connected this again is a diode connected transistor equivalent to that of a of an n MOS transistor right. So, what happens in a diode connected transistor, what is the input what is the impedance looking into the gate of a diode connected transistor the gate or the drain? In case of an n MOS it is 1 over gm. So, in case of a pMOS also it will be 1 over gm. You can actually I will encourage you to you to do it yourself once right.

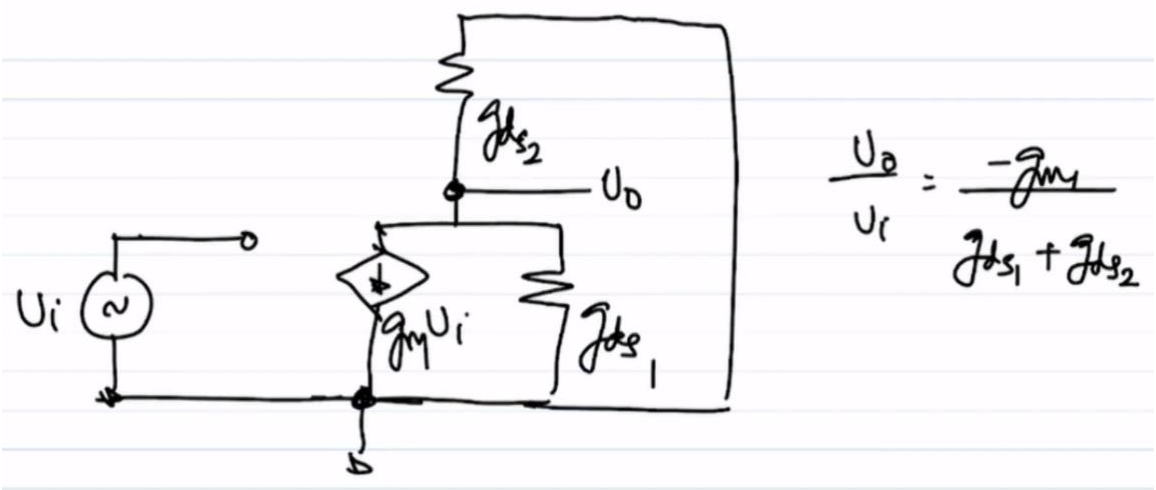


So, use the pMOS transistor use the M4 configuration diode connected configuration and find out what is the input impedance right. So, I made the statement, but you should once verify it yourself. So, this becomes a diode connected transistor, this becomes a diode connected transistor connected to the ground is 1 over gm4 right. What is the current into this terminal current is 0, if this terminal current is 0 what is this voltage VG2? VG2 is also 0 right fine. So, what is now what is left? So, we have neglected the gds right, we have neglected the gds let us put the gds of M1 back right.

So, let us put gds of M1 back here. So, this is gds1, what about this guy? This is gds2. So, let me just say that the there is a ground here. So, that I do not have to sketch the I do not have to connect the ground all the way from top to bottom every time right. So, if we had considered the gds of M4 and M3 also would it have caused any difference? No right.

So, if we had considered the gds of M4 instead of 1 instead of 1 over gm4 the resistance would have been 1 over gm4 plus gds 4, but in the end Vg2 would have been 0 right ok great. If Vg2 is equal to 0 what is its impact? What is the impact of Vg2 if it is 0? If Vg2 is equal to 0 this Vg2 is 0 which means this current source goes off correct. If that current source goes off what is the simplified circuit? What is the simplified what is how can we simplify the circuit further? This is what we should get. We have this VI right. This is gm1 minus VI, this is gds1 and we have gds2 right and this is also ground it and this is Vo right.

Everything else went off right this is the beauty of analog circuits, this is the beauty of approximations right. So, once you know how to look at how to simplify circuit then everything becomes very simple and we know we have seen this architecture multiple times what is Vo over VI? Vo over VI in this case is minus gm1 times gds1 plus gds2 right ok. So, if we had neglected channel and modulation in this case right if we are neglected channel modulation in this case the gds1 and gds2 would have been 0 and we have got an infinite gain. Now, that would have been infinitely wrong because I mean I cannot neglect a finite thing with respect to infinite right because I cannot neglect a finite thing with respect to infinite I have to put the I have to consider channel in modulation. However, if instead of gds2 if we have if we had a resistance RL and the resistance would have been much the value of the resistance would have been much smaller with respect to the rds of the transistor then I could have neglected the channeled modulation right.

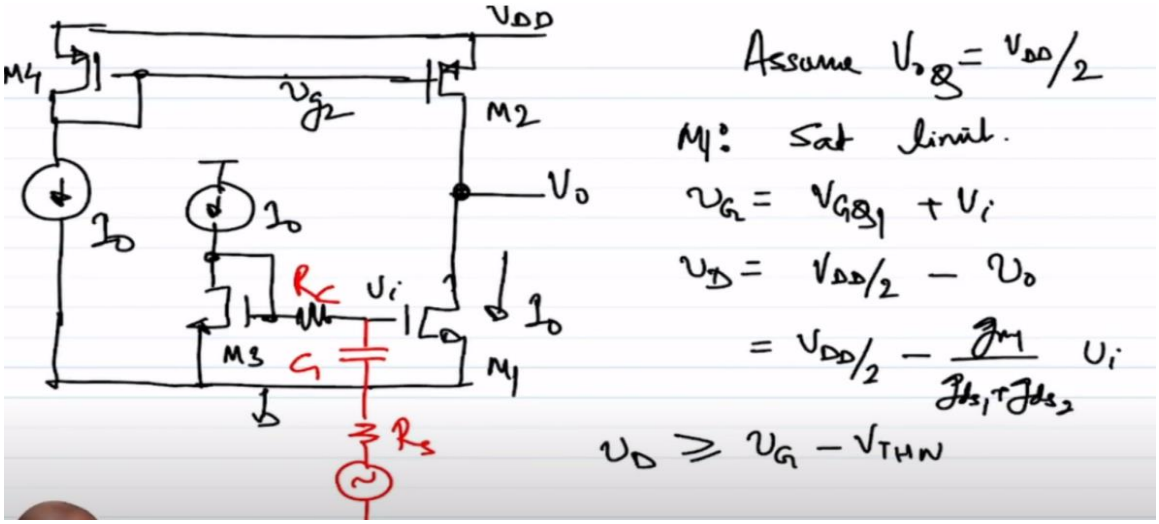


So, as you might have as you should remember is remember that it is all horses for courses right. For whichever condition we can make the approximation we should be able to make their approximation, but you should be mindful of the fact that that approximation will not hold good under all conditions right. So, that that that knowledge of that condition is extremely extremely important ok fine. So, this is what it is now if I have to find out for example, the swing limits right for this particular architecture. So, what should we do? So, let us let us do that also.

So, let me copy this guy ok. So, so if so now you see there are there are like four transistors. So, we will have to then we will have to find out the condition of the condition of linear linearity and saturation condition and cutoff condition for all four transistors right. So, let us let us start off with the with the condition on M1. So, I will do for couples and you can do the others.

So, let us do the condition for M1 right. So, what will be the condition for M1? For this we need to we have to assume something right, we have to assume something and let us assume that Vo has some quiescent voltage to start off. Again I have not told you what is the quiescent voltage of Vo right. So, let us assume that that. So, this will generally be given or the circuit will have some additional contraption through which you will be able to able to estimate what the Vo voltage will be. So, if let us assume for this particular case note that do not assume this particular thing that I am going to assume in a generic case for this particular case assume Vo quiescent to be Vdd by 2 right.

I just picked something out of the head let us say this this is being said by some other circuit which is connected across it ok. So, let us assume Voq is Vdd by 2 and let us proceed right. So, so for M1 what will be the condition? M1 what is the set limit? So, this is easy. So, if we assume that the no loading and everything on this voltage is approximately Vi I mean this quiescent plus Vi. So, what is Vg? Vg is Vgq1 plus Vi what is Vd? Vd is Voq which is Vdd over 2 minus minus gain right minus the swing this Vo correct.



What is what is Vo? Vo is is the gain of of of the amplifier times Vi. So, this becomes Vdd. So, this becomes Vdd by 2 minus gm1 by gm2 gds1 plus gds2 times Vi. So, what will be the condition? The condition for saturation will be Vd should be greater than equal to Vg minus threshold voltage n and you can plug in the values and you will get something right. Similarly, you will get the same thing for you will get something for the for the cutoff condition also, but let I would like to concentrate more on what is happening with the with the n MOS transistor because that is the new thing in our in our in our system right ok.

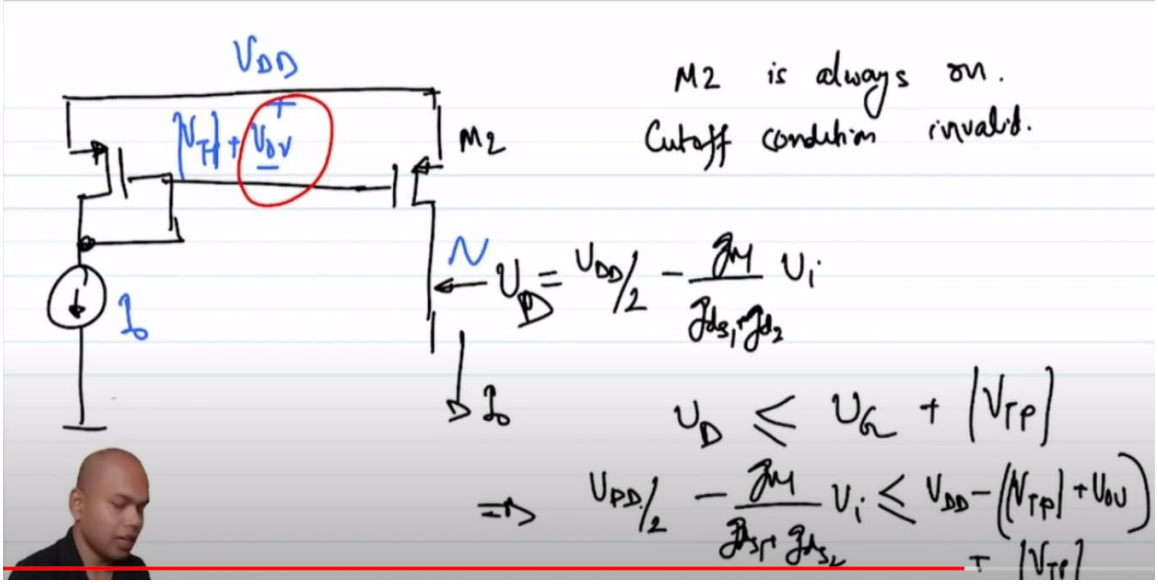
So, let us do that. So, we know that this quiescent current is Idsq right Idsq is equal to how what Idsq is is equal to Io because we have a current mirror which is which is setting into Io ok. So, so what will be the condition for this is M2. So, what is this it is this is Idsq current which is equal to Io what is the incremental current? What is the incremental current that is flow what is the incremental current that is flowing what is the how will you find out the incremental current to find out incremental current we have to go back to the our incremental picture right. So, what is the incremental current that is flowing that is gm1 times Vi right gm1 times Vi is flowing into that into the incremental load correct.

So, since gm1 times Vi is a incremental current. So, this total current is Io plus gm1 times Vi right. What is the what is this voltage what is the total voltage this is Vo right what is the total voltage total voltage is Vo over 2 sorry Vdd over 2 plus Vo what is Vo which is minus gm1 by gds1 plus gds2 times Vi correct this is a total Vo ok. So, do you think ok. So, let me ask you one question where is this gm1 times Vi incremental gm1 times Vi going this incremental gm1 times Vi going is going into into the model resistances right the incremental resistances. What is meant by model resistances what is the genesis of those model incremental resistances the genesis of that is when this drain voltage swings when the drain voltage of an nMOS or a pMOS transistor swings that drain current also changes by slight amount because of the channel length modulation right.

It is when we say that this incremental current is going into an incremental resistance what we are essentially saying is that there will be a slight change in the in the drain current right and what we essentially are trying to model what we are essentially trying to say is we will assume the transistor is ideal, but in parallel to the transistor there is an incremental resistance right and so the incremental current is then going into the into the incremental resistance right. But as far as as far as the quiescent current is concerned as far as if we neglect channel and modulation for example is the current through M2 changing the current through M2 isn't changing because this is a constant current bias right. So the Vsg the Vgs of this transistor or Vsg of this transistor is is fixed what is the Vsg of the transistor Vsg of the transistor is threshold voltage mod of threshold voltage plus overdrive and overdrive is that under root 2 I0 by mu C of W over L and so on right. So for all practical purposes I can say that this I0 is kind of constant. So if I0 is constant right then will M2 ever go into

cutoff when can M2 go into cutoff M2 can go into cutoff only when V overdrive changes right.

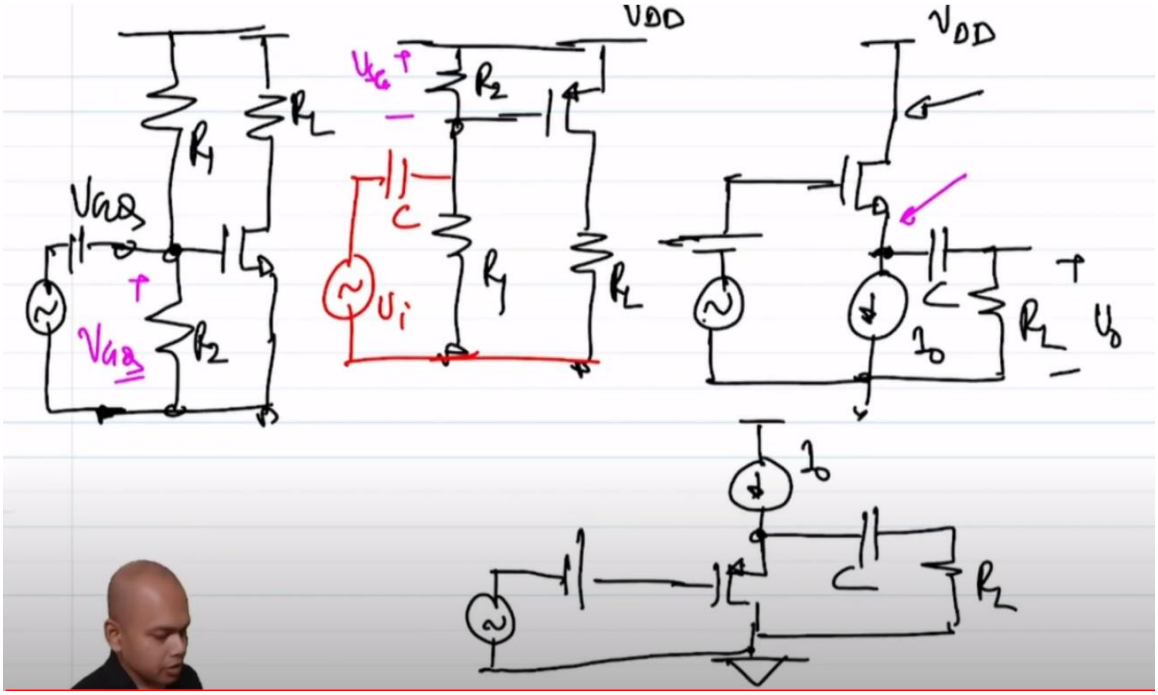
If the transistor Vsg goes towards 0 the M2 can go into cutoff but since its Voverdrive is not changing right it's fixed M2 cannot ever go into cutoff right. So M2 is always on so the cutoff condition for M2 is no longer valid right. What about the what about the saturation condition so cutoff condition invalid right. So what is the saturation condition the saturation condition will be our drain voltage that is V0 right. So let me write in terms of Vd so Vd there should be a maximum condition on Vd right.



So it means Vd should be less than equal to the gate voltage the total gate voltage plus the threshold voltage right. What is Vd? Vd is Vdd over 2 minus gm1 by gds1 plus gds2 times Vi it should be less than equal to what is Vg? Vg is Vdd minus threshold voltage plus V overdrive right plus mod of Vd right. So this is the maximum I mean the condition that you will arrive after solving this algebra will give you the swing limit that you have to honor for as far as M2 is concerned right ok. So before we end this lecture what I would like to draw your attention to is that since it looks like an NMOS and PMOS transistors are siblings right they are brothers and sisters right. So it essentially means that whatever the NMOS transistor can do a PMOS transistor should also be able to do I mean we as it turns out we started the course with an NMOS transistor but that did not necessarily be the case we could have as well started with a PMOS transistor which means all the amplifier configurations right common source, common gate, common drain, VCVAs, VCCAs, CCVAs and everything that we have done with the NMOS transistor can also be made with a with a PMOS transistor right.

So let us see quickly what is what I mean by that. So we have this so let me yeah so let us so this is the common source amplifier configuration with an NMOS transistor right. What will be the if I have to make a common source transistor common source amplifier

configuration using a PMOS transistor what should I do? I should basically replace the NMOS with the PMOS first and with the source at the higher voltage right. Here the source is fixed voltage what is the fixed voltage the fixed voltage is ground because the source is the lower terminal it has to be grounded right fixed voltage is a lower terminal voltage which is ground in case of a in case of a PMOS transistor it should be the higher terminal voltage. So this becomes a PMOS transistor the incremental grounded terminal will be that will be the source which is VDD at the drain we connect RL other side of the RL goes to ground right. So basically everything flipped right you take this guy you take this guy and flip it right.



So whatever goes in the is on the up comes down and vice versa right and you have to take care which is the source which is the ground. What should we do where should we apply the VGS? The VGS is applied between the gate and the source in case of a in case of a NMOS. Similarly the VGS has to be applied between the source and the gate and how did we apply that? We can apply it like this or we can apply it I mean in this case what did we do what were the what were the ways of applying I mean the very basic thing that we started off with was this this is R1 this is R2 this was Vgq. Similarly in this case we'll have to do so this will be R2 if we have to keep the same Vsg and same overdrive and so on this will be R1 because ultimately the voltage across R2 is Vgq we wanted the voltage across R2 to be Vsgq right.

So Vsgq. However we applying the input we were applying the input by AC coupling it into into into our configuration so in this case what should I do I can AC couple the input as well because this is AC coupled it doesn't really matter whether the VI is reference to a VDD or VI is reference to ground right. So this becomes the equivalent of the common

source amplifier in case of with a NMOS right. What will be for example a common drain amplifier in case of an NMOS what was the common drain amplifier in case of an NMOS our common drain amplifier was this. I'm not showing the input side biasing anymore right. We were taking the output here so what will be the common drain amplifier in case of with a with a PMOS right.

Basically the same thing but everything flipped up so so instead of this transits instead of the NMOS we put the PMOS. The drain of the PMOS NMOS is connected to the VDD here the drain of the PMOS will go to the ground correct. Gate is biased again I mean so we can bias it any in any of your favorite ways I am showing the most use most easy way easiest way to bias I mean obviously we know by now that this cannot be done we need other other ways of biasing. What is what is connected to the source here what is connected to the source? The feeding current out of the source right so in this case in case of a PMOS we have to feed current into the source right okay. So we can do that we can feed current into the source this becomes I0 and we were taking the output from the source of the MOSFET AC copper RL right C right.

Similarly you can you can you can sketch the common gate amplifier right and similarly you can do current mirrors right what was we already did a current mirror biasing here we did a current mirror biasing here with the PMOS. Similarly you can do cascoded current mirror biasing you can do wide swing current mirror biasing right. So what I am trying to what I am trying to get at here is that your whatever you can do with an NMOS you can do with the PMOS. So you should get used to handling a circuit independently from scratch even if you are giving you a PMOS right okay. In this upcoming assignment you will see PMOS circuits I mean the same known circuits which you have done which we have gotten accustomed to using a NMOS you will see the same circuits using a PMOS and also for those of you who will be taking the final exam of this course a spoiler is there will be questions on NMOS on PMOS and NMOS both so it makes sense to get yourself accustomed to circuits using using PMOS right okay I will see you in that next lecture. Thank you.