Course name- Analog VLSI Design (108104193)
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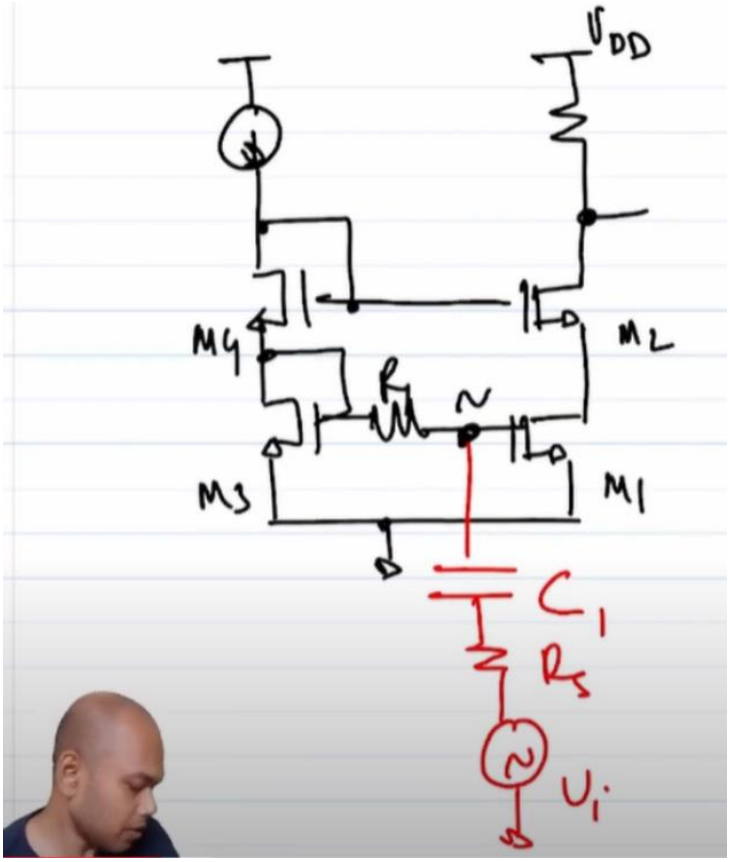
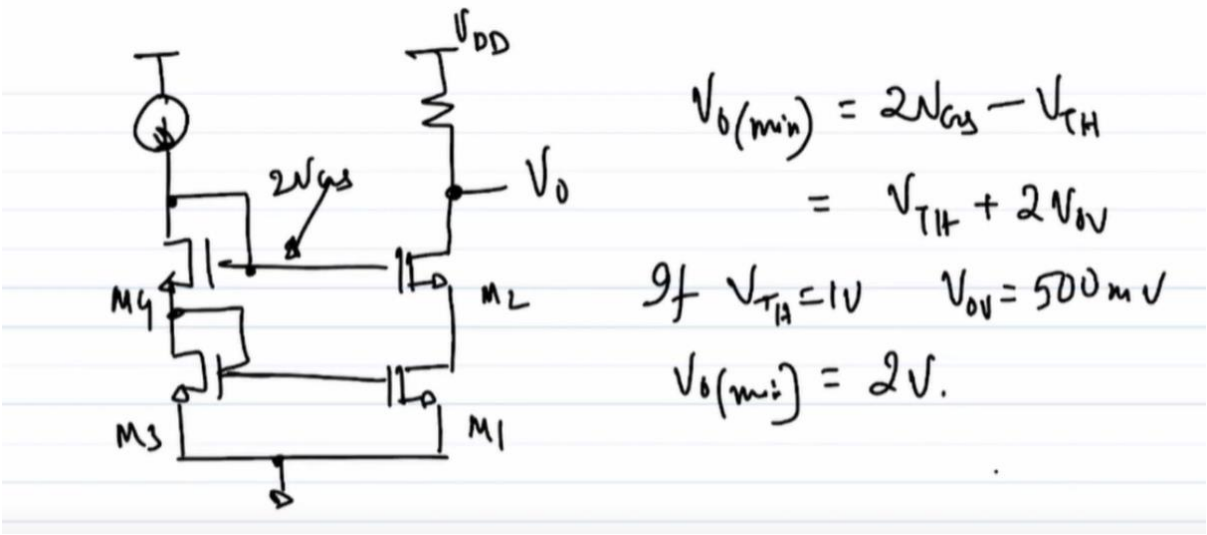
Welcome back. So, as it turns out, this is one of the popular, the one that we saw, right now, is used to be one of the popular biasing schemes for current mirror biasing. The next question that we need to ask ourselves is, how do I apply signal to this configuration, right? How do I apply signal because ultimately, we would want to take, make it like look like an amplifier, right? So what did we do in case of a common source amplifier with a current mirror bias? We found out a way of AC coupling the signal, we found out a way of AC coupling the signal to the gate of the common source amplifier, right? So we found a way of coupling our voltage source to this node and how did we do that?



We used a coupling capacitor and we can do the same thing here. So basically, this is what we did. So, this was Vi, this was Rs, then we had to size this coupling capacitor, let me call it C1 in certain ways so that almost the entire of Vi appears at the gate of M1, but that was also not possible all the time. What we had to do was do this, right? So, if we choose our values of R1, C1 correctly, then it is possible to get the entire voltage swing at the gate of M1 and then it essentially becomes the same old common source amplifier topology but now with a cascode

configuration, right? Okay, fine.

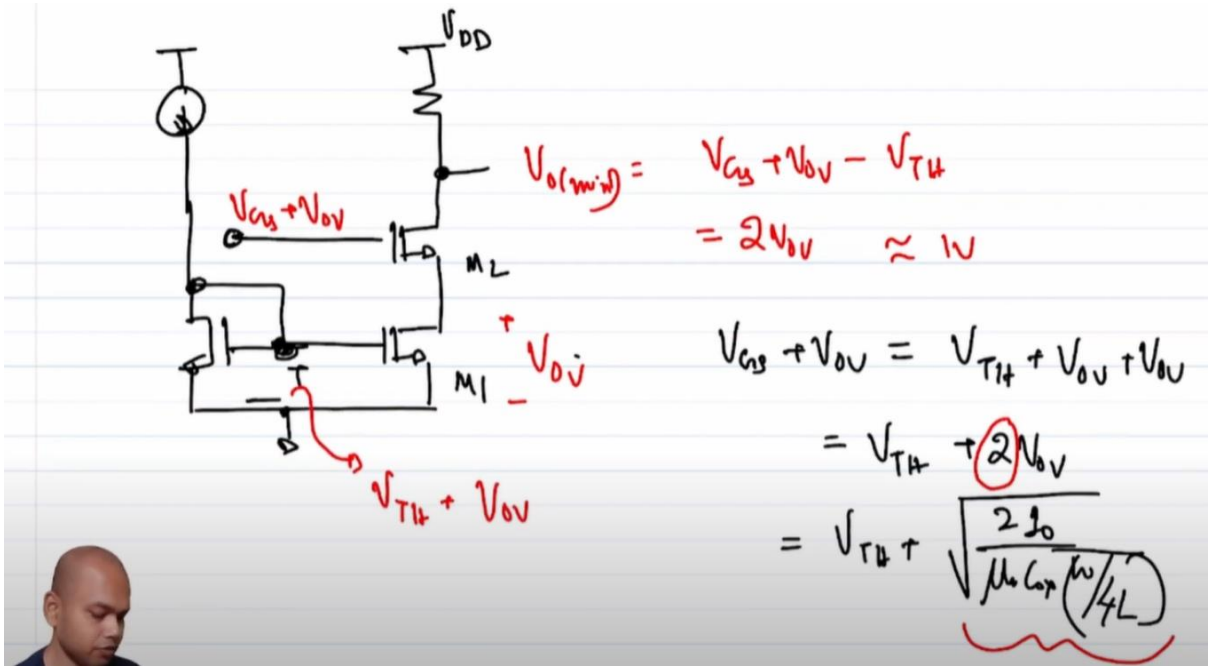
So now the one that we, the stuff that I want to draw your attention to is the following. So let us only concentrate on the bias part of it with assumption that we know how to, AC couple the input and the output. Okay, so this is M1 and so on and so forth. So, let us say this is V0, what is the minimum V0 that we have while keeping both M1 and M2 in saturation? If we keep on reducing V0, which transistor is going out of saturation first? Note that this current is largely unaffected by the change of V0, right? Since this current is largely unaffected by the change of V0, then we can essentially say that if I reduce V0, then the transistor M2 is likely to go out of saturation, right? So, to establish that we needed to figure out what is the voltage at the gate of M2 and that is quite straightforward because now we know that this voltage is 2Vgs, right? So, what is V0 mean? V0 mean, so minimum allowable voltage of V0 is 2Vgs minus 1 threshold voltage, which is effectively equal to $V_{th} + 2V_{OV}$, right? So, this is much higher than the minimum voltage in a common source amplifier without all this cascode configuration, right? So for example, if let us say threshold voltage is 1V and overdrive is 500 millivolt, right? Then V0 mean effectively becomes 2V.



Now when you are operating from a supply of let us say 3V or 3.3V battery, then this can be a problem. You are essentially saying that the output cannot swing below 2V, then substantial portion of the available output voltage is lost just to ensure that our transistors are biased properly. However, if we say that we will not do this, let us do this, let us say forget about these-type, of biasing, right? So let us forget about these-type of biasing. So, and I bias this with let us say some Vgs, right? What is the minimum voltage across M1 that I need to maintain? Overdrive voltage of M1, right? While the voltage across the Vds of M1 is equal to V overdrive, what is the minimum voltage that I need to maintain at the gate of M2? This should be Vgs plus V overdrive, right? So, what will be the minimum voltage at V0? Minimum voltage minimum allowable voltage at V0 will be V0 mean will be Vgs plus V overdrive minus one threshold voltage, which is equal to 2V overdrive, right? So, which can be 1V with the example that we, what we just took, right? in the previous page?

So definitely you see that if you have supply voltage limitations, then clearly if we can arrange our biasing circuit such that these conditions are met, then I can essentially allow the output to swing at a far lower much closer to ground than I could have otherwise, right? So then, now, the question is how do I get these voltages? Now 1 Vgs is easy to get. So this is easy to get. We can get Vgs like this. Okay? But how do I get the other one? One $V_{GS}+V_{OV}$. Essentially what I am asking is, how do I get this voltage of $V_{GS}+V_{OV}$ using transistors? and current sources not by register divider, not by register divider methods, right? So let us see.

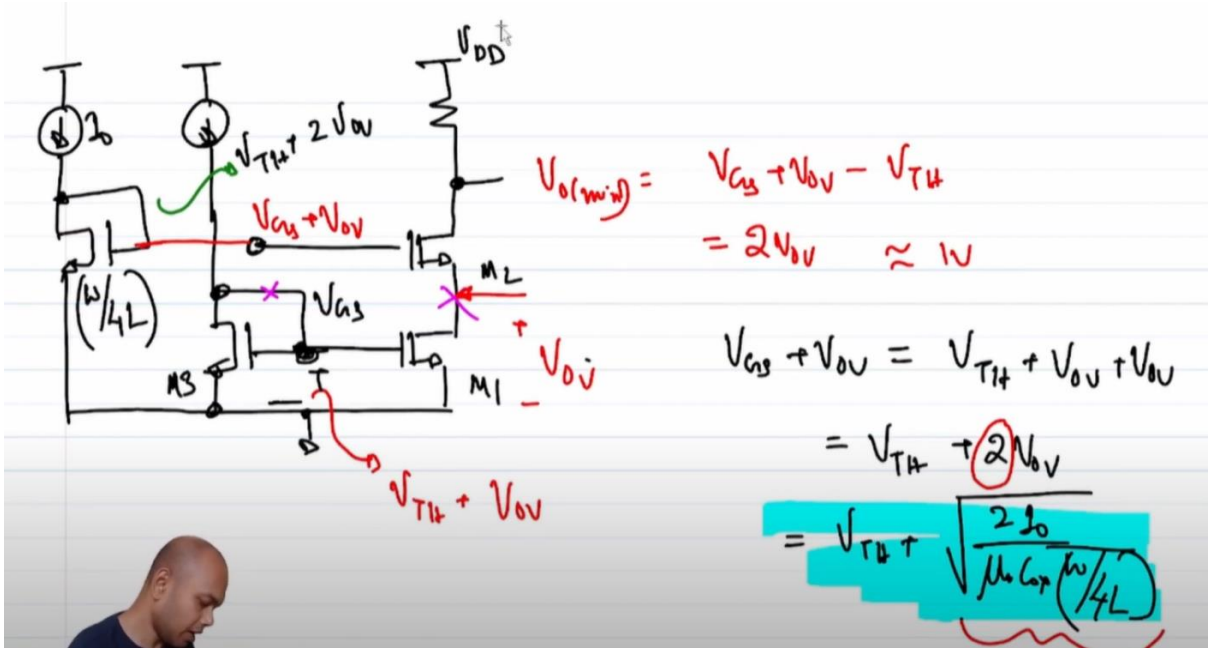
So, what is $V_{GS}+V_{OV}$ is equal to if I spell it out, this becomes 1 Vgs becomes $V_{th}+V_{OV}$ and we have another V_{OV}. So, this is $V_{th}+2V_{OV}$, right? Now we know how to generate $V_{th}+V_{OV}$, right? So, because this is $V_{th}+V_{OV}$, but here we need $V_{th}+2V_{OV}$. So, how should I go about thinking about it? Now, the trick to this is to recognize that the overdrive voltage is a function of W by L and I not, right? So, let us see if I expand this, this becomes $V_{th}+2V_{OV}$ is $2\sqrt{\frac{2I_o}{\mu_n C_{ox}\frac{W}{L}}}$, right? And if I take these two inside, so this becomes $\mu_n C_{ox}\frac{W}{4L}$, right? Note that, so what does this remind you of?



What does this second term remind you of? It looks like this is a diode-connected transistor having a threshold voltage of Vth whose current is I not, but it is $\frac{W}{L}$ is, now $\frac{W}{L}$ is $\frac{W}{4L}$, right? So essentially this looks like a transistor, this looks like a case where I have this, I have I not and that one, this is $\frac{W}{4L}$, right? So, what will be this voltage? This voltage will be equal to this guy, right? So, this becomes $V_{th}+2V_{OV}$ and now that we have it, what we can simply do is

connect these two together, right? So, this is again one way of biasing, right? Since this is one way of biasing, so this seems to, this seems to have solved the problem that we are facing in the previous architecture where we had two diode-connected transistors stacked on top of each other to generate the requisite voltage, but the problem was the output, the minimum output voltage would have been, would have been, would not have been as low as it could have been. But do you see a problem with this architecture? Not a problem per se, but do you see something that can go wrong with this architecture? I am sure some of you might have already figured this out. The problem here is the minimum voltage at, what is the voltage at this, at this node at the source of M2? The voltage is Vov, V overdrive.

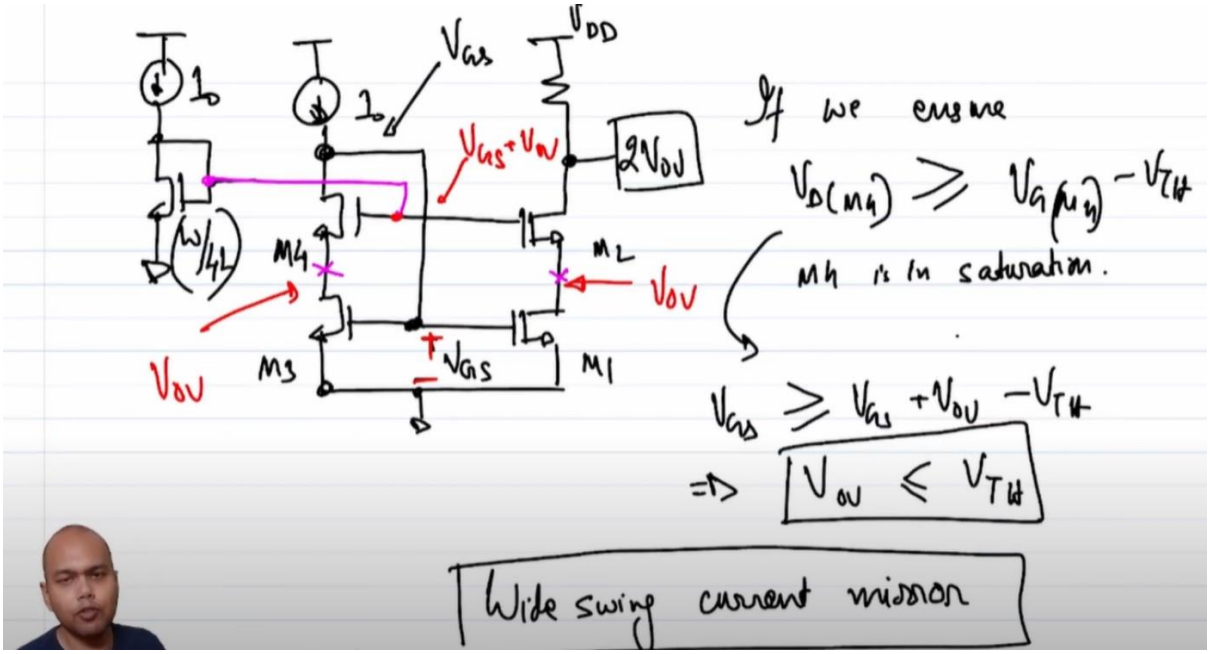
What is the voltage at the gate or rather at the this is M3. What is the voltage at the drain of M3? This is Vgs. So, these two voltages are not identical anymore, right? So, this voltage and this voltage are not identical anymore, which means the mirroring of current between these two branches will not be accurate, will differ slightly. So, these-type of biasing are okay as long as you are not looking for exact biasing, exact mirroring, but you are looking for wide swing and high output impedance. However, if you are looking for exact biasing, then this also needs to be modified a bit.



So what I will show you next is an architecture which does the, which does exactly that. Due to lack of time, I will not be able to show you the derivation, but you can analyze it yourself to convince yourself that this indeed is the case. So, what this network does is basically, make this up a bit. This is basically diode-connected M3 from top, right? So, this remains Vgs, but now I have a possibility of biasing this node in such a way that these two nodes that the drains of M1 and M3 are identical. As it turns out, you can do that using our good old diode-connected transistor having aspect ratio of $\frac{W}{4L}$.

And we can see right here we can quickly have an understanding of why this works. So, if this

is Vgs, what is the minimum voltage at the drain of M1 while keeping M1 in saturation? This will be V_{OV}. What is the minimum voltage at the drain of M4 while keeping M3 in saturation? This will also be V_{OV}. So, what is the voltage that is required at the gate of M4? This will be $V_{GS} + V_{OV}$, which was similar to the earlier case and that is why you have, that is why we have this architecture. And what is the voltage now at the drain of M4? What is this voltage? This is Vgs.



So as long as, so, if we ensure the drain voltage of M4, So, $V_{D,M4} \geq V_{G,M4} - V_{th}$. We have saturation condition for M4, which means that we have M4 is in saturation. So, which means what we need to ensure? We need to ensure V_{GS}, $V_{GS,M3}$, but if we assume all the sizes are identical, everything is $\frac{W}{L}$, so Vgs is greater than equal to V_{GS} plus V overdrive minus threshold voltage over code, which means we all, we are looking for is a case, where we are sizing V overdrive at a voltage which is less than the threshold voltage. So, as long as, we, as we honor, this condition of $V_{OV} \leq V_{th}$, then all transistors will be in saturation and the mirroring will also be accurate and the minimum voltage at the output will be V overdrive. So, that is why this particular configuration is often called Wide-Swing current mirror.

Very popular circuit, quite useful especially in low voltage design where every 100 millivolt can be a significant portion of the power supply. I mean for example, in today's modern technologies, we operate with a Vdd of let us say 1 volt, 1.2 volt, and the threshold voltages are still of the order of 300, 400 millivolts. So, if you bias, if you lose one threshold voltage, one threshold voltage essentially is a significant portion of, is almost like 30 per cent of the available signal swing, so you cannot do that, right? So that is why all networks or circuits which enable us to give, which enable us, a lot of room for the output signal to move is often, often preferred. Thank you.