Microprocessors and Interfacing
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Lecture – 27
Modes of 8254

In the last class, we are discussing about the modes of 8254. So, we have discussed the first three modes: mode 0, which is interrupt on terminal count. Mode 1 programmable one shot and mode 2, rate generator; see next one is mode 3; mode 3 is square wave generator.

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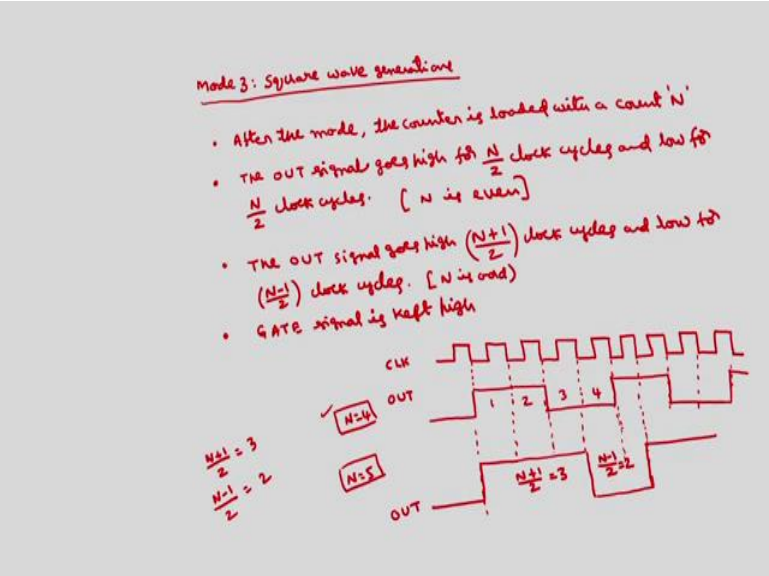

We can generate this square wave using 8254. In earlier lectures we have discussed about this square wave generation using, software also. We can using 8255. But the difference is as I have told in the last lecture also. So, using 8254 we can generate the accurate delays. If you want to generate a square wave with 1 kilo hertz, if I use 8254, the accuracy will be more when compared with the generation of the square wave using any other techniques such as 8255 and all.

So, in this square wave generation, after the mode set, once the mode is set by using that control word register the counter is loaded with a count of N. So, once the mode is set the counter is loaded with count N. Then once the count is loaded into this counter, the out signal of this particular counter is say I mean, counter is having one OUT signal.

OUT signal goes high for N by 2 clock cycles and low for the remaining N by 2 clock cycles, and the same process will repeats. This is the case if N is even. N can be odd also. See in case of N odd the OUT signal goes high for N plus 1 by 2 clock cycles and low for the remaining which will be N minus 1 by 2. And their GATE signals will be kept high.

See these are the different points related to mode 3. So, if I take the wave forms if I take the clock wave from here, this is clock of any particular counter you have three counters you can use any of these counters, you can program in mode 3. With respect to this clock, how would this output will varies OUT signal for the both the cases N is even as well as N is odd.

High signal I mean GATE signal I am not showing, which will be high. This is clock signal. Then the OUT signal, will be high for N by 2 clock cycles and low for N by 2 clock cycle, in case of N is even where as in case of N is odd, high for N plus 1 by 2 cycles and low for N minus 1 by 2 cycle. First I will draw for high, I mean sorry N is equal to even. So, we know that the changes occurs at the negative edge of the clock, as I have told there are 3 counters, 16 bit pre settable counters, down counters, which operates on negative edge.

Suppose, if I take OUT signal for N is equal to say 4 even number, then this will be on for 2 signals this will be on here 1 and 2. Then off for 2 signals, the same thing will repeats. This is OUT signal if N is equal to 4, this is if I load N with 4, this is 1, 2, 3, 4 now 0,1,2,3. OUT in case of N is equal to 5, which is odd.

So, for N is equal to 5, what is N plus 1 by 2? N plus 1 by 2 is 6 plus 1 by 2 is 3 N minus 1 by 2 is 2. So, 3 plus 2 becomes 5. So, this OUT signal will be high for 3 clock signals and low for 2 clock signals. 1,2,3 high then, low for 2 clock signals, then again high for 3 clock signals, so on.

This is for N plus 1 by 2, which is in this case 3 this is N minus 1 by 2, which is 2 in this case. This is 1 clock signal, 2 clock signals, 3 and this will be 1, 1 clock signals and 2 clock signals. This is 2 clock signals it will go to low up to, second clock signal then high. So, this is about the mode 3 of 8254.

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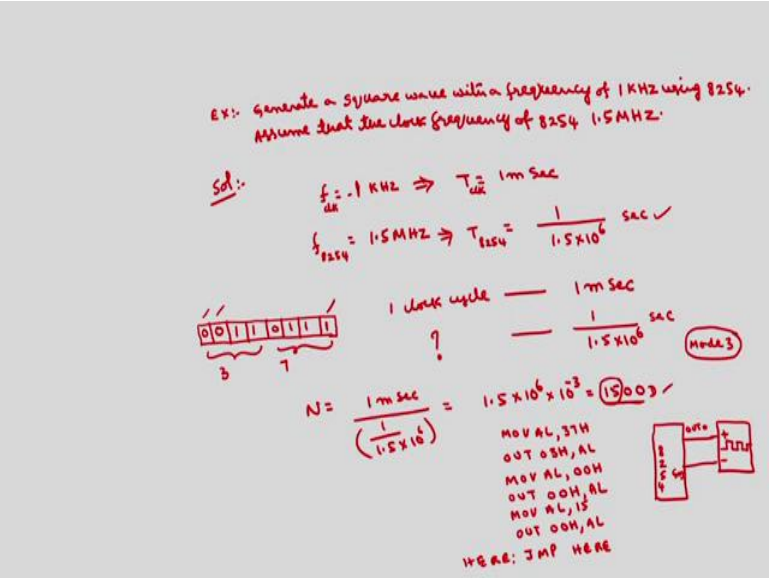

So, if I write a program let us take an example. Generate a square wave with a frequency of 1 kilo Hertz using 8254. Assume that the clock frequency of 8254 is 1.5 mega Hertz.

As I have told in the last class, the clock frequency of 8254, we can vary from DC to 10 mega Hertz. Here I am considering 1.5 mega Hertz. So, to write what is the solution for this problem, I have to generate 1 kilo Hertz signal. So, frequency of the signal that is to be generated is, 1 kilo Hertz, implies time period is 1 millisecond right.

So, the clock frequency of 8254, this is clock. You can call CLK. Frequency of 8254, is 1.5 mega Hertz implies what is time period of 8254 clock is, 1 over 1.5 into 10 raised to the power of 6. These many seconds. So, in order to generate this square, wave using this 8254 in mode 3. So, we have to load this counter with appropriate value. So, that if N value is even number it will be on for N by 2 clock cycles, off for N by 2 clock cycles.

So, how to find out the N value? So, what should be the value of N? To produce this frequency of 1 kilo Hertz square wave, if I connect that OUT signal to the CRO. So, for that in order to find out the N value capital N value 1 clock cycle of the clock is equivalent to 1 millisecond. 1 clock cycle is equal to 1 the millisecond duration. Then what is the duration that we want? We want a duration of 1 by 1.5 into 10 raised to the power of 6. For this seconds, how many clocks we require? That is the N value.

So, this will be the number of clock cycles N will be, 1 millisecond divided by 1 by 1.5, into 10 raised to the power of 6. This is equal to 1.5 into 10 to the power of 6 into millies 10 raise to the power of minus 3. So, this is equal to 1500. So, if I load this N value with 1500, if I take the decimal. So, I have to operate in as a, BCD counter. Then we can generate a square wave with the frequency of 1 millisecond at the OUT signal.

So, in order to load this value, what will be the program? Program for this one will be MOV AL, what should be the control word? Because I am using as BCD counter and I am using in mode 3 and count is 16 bit ok. So, if I form this control word register, this last bit is 1 for BCD counting, next 2 positions are next 3 are for mode selection.

So, mode 3 means 0 1 1 next 2 are RL 1, RL 0. Because you have to load 16 bit number BCD number. So, this will be 1 1, 0 0 is latching 0 1 is lower order 8 bits, 1 0 is higher order 8 bits, 1 1 is 16 bit in that first it will load a lower order 8 bits, then it will load higher order 8 bits. And this is select counter I can use any counter, if I use say counter 0 0 0 this will be 3 7 H. OUT the address of the counter register is 0 3 H per the interface connection that we have shown in the earlier class, AL this is mode set. After that we have to load this count value, on to the counter 0 because here you have selected counter 0.

For that you take the lower order values of the count, into AL 00H then OUT on to counter 0, whose address is 00H , AL. Counter 0 l is address is 0 0 counter 1 is 0 1, counter 2 is 0 2 and control word is 0 3. For the connections that have shown in the earlier lecture. Then you load MOV AL , the higher order 8 bits of the count is 15, 15 OUT 0 0 H , AL. Here you will give 15; because we have set this as BCD counter 15 will be not be taken as a hexadecimal, it will be taken as decimal.

Now we have loaded this so you have to just jump here itself. So, if you executed this program and if I connect this 8254 OUT 0. This is OUT 0 because I have used this counter 0, OUT 0 to CRO you can observe a square wave with the precise accurate frequency of 1 kilo Hertz. This we have to connect to positive terminal negative terminal of this has to be connected to the ground signal of 8254.

This is how you can generate square wave with a accurate time delays? Accurate frequencies. This is about mode 3, the next mode is mode 4, software triggered strobe mode 4.

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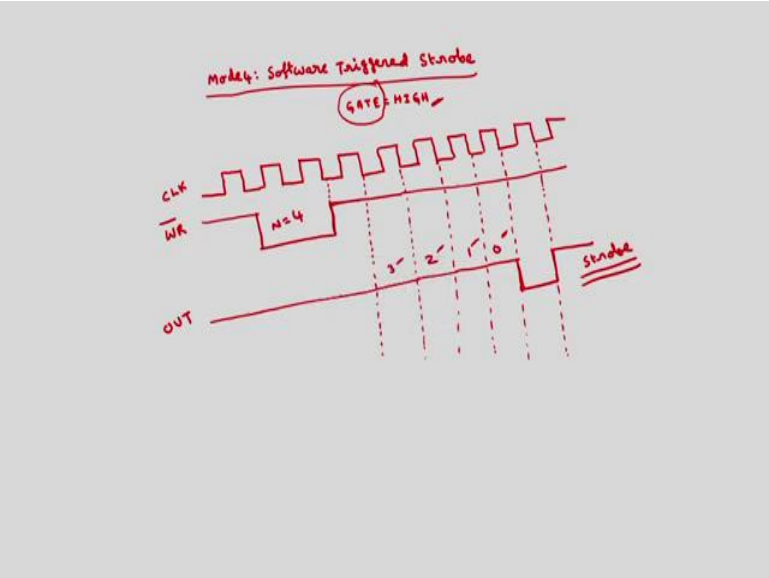

Software Triggered Strobe. So, in this case also GATE signal will be kept HIGH after the mode set, we have to load the count value on to the counter. These two points are same as that of the previous mode. Once the count is loaded into the counter then what happens is, this OUT signal will become high for N number of clock cycles.

Then it will go to low for 1 clock cycle and will acts as a strobe signal, then again it will go to the high ok. These are the wave forms for mode 4. So, if you observe the wave forms the operation will be understood, this is clock signal. If I take same N is equal to 4 this is clock I can use any of the counters write bar.

This is write bar signal, now am I showing N is equal to 4. Once this N value is rotated into the counter from the next negative edge onwards you see the next negative edge. This is negative edge the OUT signal remains high, for N clock cycles and then goes low for 1 clock cycle. So, this will be initially high only. So, from here this is 1 clock cycle, 2 clock cycles, 3 clock cycles, 4 clock cycles. Then it will go to low for 1 clock cycle, then again it will become high.

This is 3,2,1,0 then it will high for 1 clock cycle. This is OUT. So, why the name software triggered strobe? Is this signal can be used as a strobe signal, in many applications and why this is software triggered? The count is going to trigger the strobe; whatever the count that we are going to load here, this is going to acts as a trigger for this strobe. That is why the name software triggered strobe.

And we have the last mode which is hardware triggered; instead of this count we can use the GATE signal to trigger the strobe. So, GATE signal is a hardware pin hardware signal because there is a pin correspond to GATE. So, the exact the operation is exactly same, except for that here instead of using this count to trigger the strobe in mode 5 we are going to use GATE to trigger the strobe. So, the last mode is mode 5 hardware triggered strobe.

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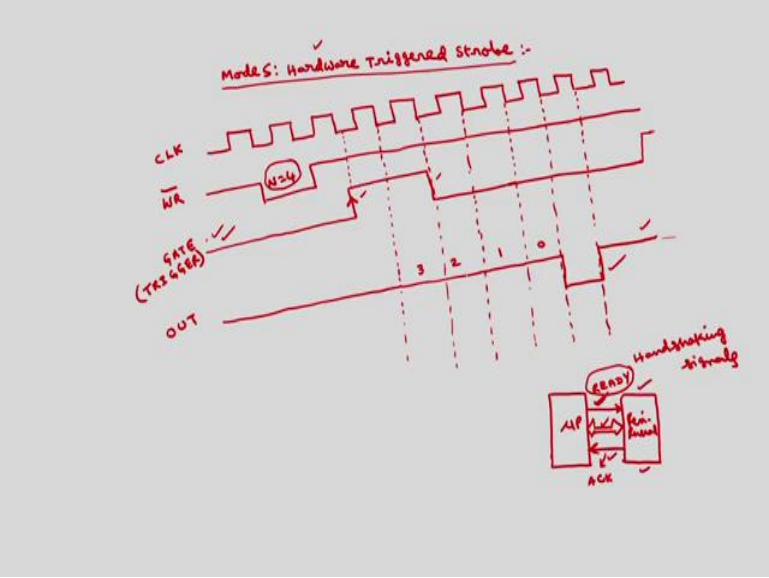

Mode 5 is hardware triggered strobe. Here also after mode set you have to load the N value on to the counter, then after loading the count, if this high I mean GATE signal goes low to high transition. Then this OUT signal will count for N clock signals once it remains high for N clock signals, then goes slow for one clock signal and the same process will be repeated. This is clock signal and this is write bar signal, I have to give the count say N is equal to 4 only then GATE signal which will acts as a trigger signal here is to be give as transition from low to high.

And it will remain high after sometime again it will be go to the low. So, once this low to high transition is occurred, the immediate negative edge onwards this is the negative edge. This occurred here say to the next thing negative edge is this, this can be of any duration. This is third clock signal, this is fourth cycle for the 4 cycles it will be high and for 1 cycle it will goes low similar to the previous mode this is OUT initially high.

It will remain high after the negative edge which follows this low to high transition of gate then will remain high; it will remain high only for N clock signals, for N clock cycles; where N is equal to 4. So, 3,2,1,0 then it will goes to low for 1 signal clock signal so this will acts as strobe signal. This is the OUT.

So, here because this strobe will be triggered by this GATE signal GATE is a hardware signal, there is a pin correspond to GATE that is why the name hardware triggered strobe. So, once if a GATE again goes from low to high transition, automatically same N value of 4 will be recorded into the counter, again it will remains high for 4 clock cycles then goes to low for 1 single clock cycle like that the process will repeats. So, this is mode 5. So, this strobe signal will be useful whenever you want to I mean a connect a slow peripheral with microprocessor. So, the strobe signal will acts as a handshaking signal, hand shaking signal is something like if I want to transfer the data between 2 devices say microprocessor and peripheral.

So, initially the signals will be exchanged between these two, before the data transfer will takes place. Initially the microprocessor will request through this signal to get ready because normally the peripheral is slow device whenever the peripheral is ready, it will send the acknowledgement through this one acknowledgement signal that data is ready. After that the data transfer will takes place.

Before the actual data transfer the signals has been exchanged. So, these two signals this signal and this signal are called handshaking signals. Why the name handshaking is? When 2 persons meet, so they will first shake the hand after that they will exchange the conservation, whatever this they want to I mean a convey the information, that information will be conveyed.

So, that is why the name handshaking signals. So, in such applications where the handshaking signals are required. We can use this strobe signals either it can be hardware triggered strobe or software triggered strobe so this is all about 8254. See you have discuss about the block diagram of 8254, then we have discussed about the control word register format the interfacing of 8254 to 8086 then different operating modes of 8254.

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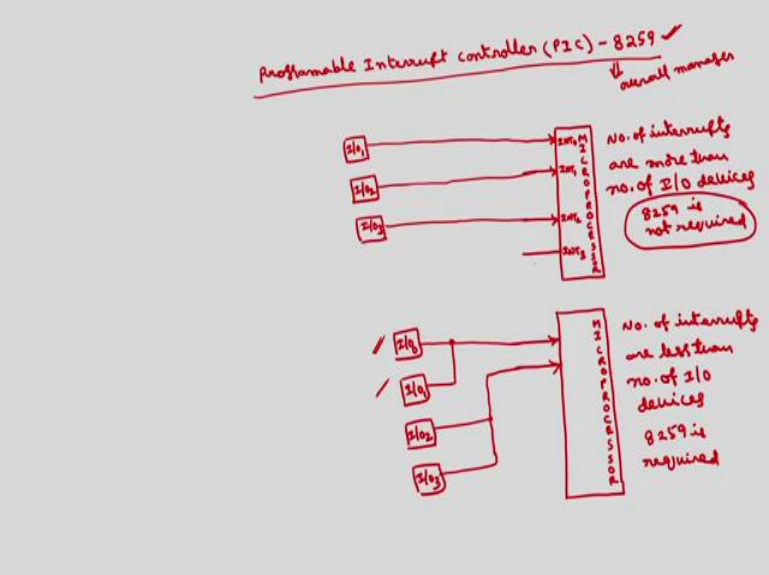

See next peripheral device is 8259 is called Programmable Interrupt Controller, called PIC the IC number is 8259. That is exclusive IC 8259, which will acts as programmable interrupt controller. First of all, what is the need of this programmable interrupt controller? So, we know that the microprocessor can be interrupted through the device, I/O device this is microprocessor it can be any microprocessor 8086 say ok.

So, I can connect the different I/O devices, we can have a number of I/O devices. This is I/O 1, I/O 2 and so on. Suppose the number of interrupts of this one is more than or equal to the number of I/O devices, suppose if I have 3 interrupts of course in 8086 we have 2 interrupts only I will call otherwise general microprocessor. First I will explain the concept so I will just call as general microprocessor because this 8259 is compatible with 8085, 8086 and some other microprocessors also.

Suppose if I have say 4 interrupts and 3 devices I can nicely connect this I/O devices to one of the interrupts of this one, this is INT 0 say INT 1, INT 2, INT 3. So, in this case there is no I mean conflict, there is no conflict because the number of interrupts are more than the number of I/O devices see when does this problem arises is, if you have the number of interrupts less than the number of I/O devices. This is the case where the number of interrupts are more than number of I/O devices.

So, if I take the second case where the number of I/Os are more than number of interrupts. Suppose if I have only 2 interrupts and I have say 4 I/O devices. Then you have to connect at least 2 I/O devices to each interrupt. I have to connect these two to the

same interrupt; similarly you have to connect these two to the same interrupt. In that case you have to assign the priority and you have to resolve the problem. So, in order to resolve this problem where if the number of interrupts are less then number of I/O devices.

So, you have to resolve the priority problem and you have to interact with the microprocessor. There should be some sort of a mediator is required between the I/O and microprocessor which will manage the efficient use of these interrupt system ok. So, that manager is this 8259. 8259 will acts as overall manager between the I/Os and the microprocessor.

So, this will perform the various tasks like assigning the priority to the I/O devices, the one with highest priority will be served first after that remaining will be kept pending. So, all of these operations will be performed by this 8259. This 8259 will acts as the overall manager between the microprocessor and I/O devices. Here 8259 is not required because number of I/Os are less than number of interrupts where as in the second case 8259 is required to resolve this problem of conflict between the different I/O devices.

So, what is the first block diagram of 8259? So, how this will resolve the problem? So, we will discuss in the next slide. So, if we come for this block diagram of 8259 this is 28 pin IC, the different signals that are available on this 8259 are shown on this architectural diagram.

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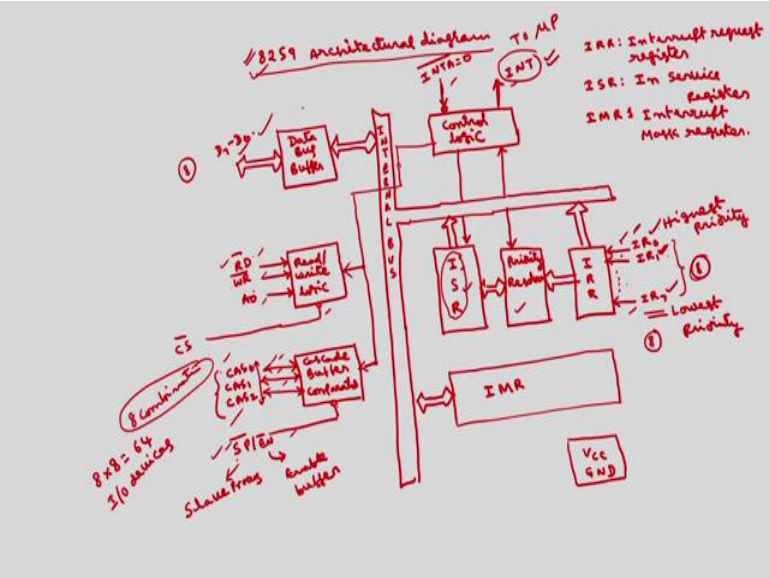

So, if you consider the Architectural diagram of 8259. There will be some internal bus, this is internal bus. So, which will be easy to communicate between the different blocks of 8259. So, the main important blocks are there is some control logic, control logic then we have for this control logic we have INTA bar and INTR. There are two signals which is called INTR, I will explain the functions of all these signals in detail this is INTA bar.

INTA bar is active low signal so I have placed a bubble here. Normally, a bubble represents active low signal. And then we have interrupt request register through which each interrupt can be used to serve 8 I/O devices. Here is 1 block called I interrupt, this block is Interrupt request register IRR, I will write the abbreviations here IRR is Interrupt Request Register.

I will explain the functions of this will be having 8 signals IR 0 to IR 7. So, each interrupt can be connected to 7-8 I mean I/O devices through this IRR because if all these interrupts occur simultaneously, then you should have some circuitry to resolve the priority of the this interrupts, so there is a priority resolver. Then we have in service register which keep the record of the serviced interrupts in service recorder register ISR is In Service Register.

So, this will be connected to the internal bus. So, this is the connection between the control logic and these 3 blocks, then we have interrupt mask register so we have to mask some interrupts, whenever more than 1 interrupt request to the use of this interrupt of 8086 or any microprocessor, there is a Interrupt Mask register. So, there are total now here 8 signals here 2 signals total 10 signals and we have similar to this 8254 there is a data bus buffer; which will be easy to transfer this control signals and status signals of 8259 with the microprocessor data bus buffer. So, it is a 8 bit data bus which has to be connected to the data bus of 8086 D7 to D0.

Then we have read-write logic which is also similar to 8254 read-write logic here will be having chip select signal A0 signal this is chip select signal read bar signal, write bar signal these are common with 8254 also. But 8254 we have A1 and A0 whereas here we have only A0, A0 in connection with read bar, write bar signal will be easy to select the different registers inside the 8259.

There is cascade buffer we can cascade one of the future of this 8259 is we can cascade three 8259's together cascade buffer comparator. So, this is I am also having 3 signals, this is having 3 signals CAS 0, CAS 1, CAS 2.

Then we have one active low signal which is called as SP slash Enable these are 2 active low signals. So, SP stands for Slave Priority, EN stands for Enable Buffer. So, there are total 28 signals there 8 signals here and this 8 signals here, 16 signals then 2 signals here 18, 19, 20, 21, 22. 23, 24, 25, 26 and there are 2 signals VCC and ground, this 8259 is a 28 pin I C.

So, if you come for the function of different signals, say whenever the I/O device which is connected to one of the interrupts of one of these lines of this IRR register. So, this will be connected to one of the I/O device, this will be connect to one of the I/O device, this will be connected to one of the I/O device. So, at a time 8 I/O device can be connected through these lines.

So, what this IPR will do is so whenever the request comes, so it will store it will give this as a highest priority in case of normal process and there is one process called rotating priority where we can program the priority of IR 0 to IR 7. So, in the normal case this is highest priority and this is lowest priority. So, the signal that will be received through these IR 0 to IR 7 will be resolved it will be assigned some priority, then the one which has to be processed is given to the ISR. So, How does this interrupt will be processed?

So, corresponding to each interrupted will be having one interrupt service sub routine. So, whenever the microprocessor is interrupted through this will be connected to the Microprocessor. So, whenever the microprocessor receive this interrupt the microprocessor controller will transfer to the interrupt service sub routine ok. So, when How does this interrupt for the microprocessor will be enabled?.

So, based on these 8 requests this will resolve this problem and the one with highest priority will be considered and that will be stored in ISR; then after assigning this highest priority this 8259 is complete 8259 will request the at microprocessor through the signal INT signal, for the use of that the interrupt of 8086. Once the microprocessor is ready to accept this interrupt it will acknowledge through INTA bar once this INTA bar becomes

0; so they interrupt branch address of that particular interrupt will be placed on to the data bus.

So, the microprocessor control will goes to that address now it will perform whatever the task that is required for that particular interrupt, then the last instruction of the interrupt service of routine is Ireturn interrupt return it will come back. Then the device with this next priority will be recognized and the corresponding address will be generated by this ISR and that will be placed on to the data bus. The microprocessor control will goes to the that particular service of routine now it will resolve.

In that way we can process 8 I/O devices, if I use single 8259. Whereas as I have told here cascading of 8259 is also possible if I cascade 3, 8259's, then what happens is, corresponding to each 8259 eight devices we can control ok. So, using this 3 we can have 8 combinations so you have 3 bits means 8 combinations 8 combinations and correspond to each combination we can have 8 devices.

So, totally we can have 8 into 8, 64 I/O devices can be connected in cascade mode, 64 I/O devices can be connected if I use this cascade mode, because of these 3 bits 8 combinations and in each combination we have 8 different signals. So, total 8 into 8, 64 I/O devices can be connected to this 8254 and this read bar. So, whenever this microprocessor want to read the status of this 8259 registers.

So, this read bar will be 0 similarly write bar means the microprocessor will write something. So, A0 in connection with this read bar and write bar will be used to select the various registers. So, these are the I mean functions of this there is a slave processor mode so this will be used in cascading modes so enable buffer So, how this 8259 will be cascade? We will discuss later.

So, these are this signals are basically cascading signals and this is also used for because this is connected to cascade control this I mean SP bar by EN bar. So, this is about the overall function of 8259 similar to 8254, 8255 here also we have some control word registers by programming the control word registers; we can control the operations between 8259 and 8086. So, the details of the control word registers and how this control word registers can be programmed to service the I/O requests? We will discuss in the next lecture.

Thank you.