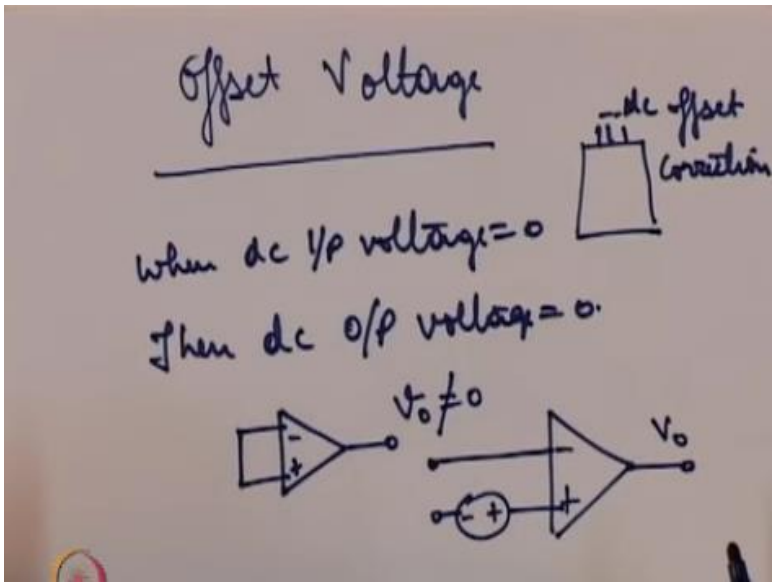
Analog Circuits
Prof. Jayanta Mukherjee
Department of Electrical Engineering
Indian Institute of Technology-Bombay

Week -02
Module -02
Non-Idealities in OPAMPs (Offset Voltage and Bias Current)

Hello, welcome to another module of this course analog circuits. In the previous module we had covered the non-idealities or we have just introduced to some of the non idealities that are present in an opamp like finite bandwidth, finite gain and also the what is known as the slew rate? In this module we should we shall consider some more of these non idealities so one more non ideality that designers face when dealing with an opamp is what is known as offset voltage?

(Refer Slide Time: 00:52)

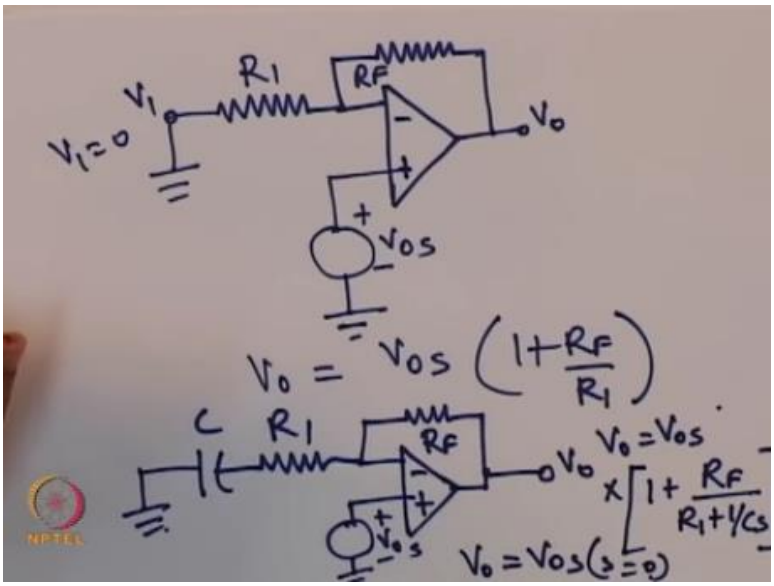


We call in the first lecture I had mentioned that when you have a fan chip, there are some pins allotted for dc offset correction, so this correction is related to this concept of offset voltage. Now ideally when dc input voltage = 0 then dc output voltage should also be = 0, so in other words if we have an opamp connected like this Vo should be = 0 but in reality, this is not see this is what is known as offset voltage.

So, we can model this like this you know we have a opamp with a certain offset voltage present okay and this kind of appears at the output the problem with this is that in an inverting

configuration this input offset voltage gets amplified like this inverting amplifier will be like this.

(Refer Slide Time: 02:21)

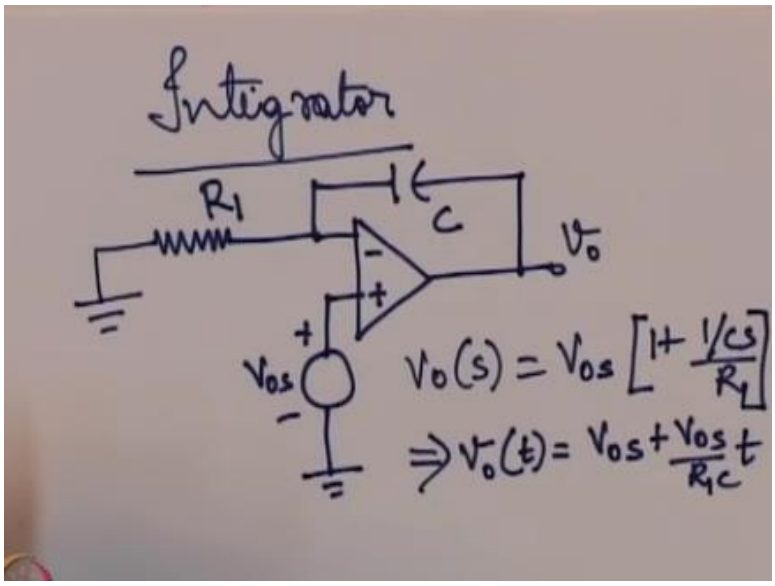


Or even if suppose this we ground so V1 = 0 then what happens is that Vo is simply = Vos 1+ this is Vos is in the non inverting configuration so we have an output voltage which is like this and the problem is that this Vos is now amplified by this factor easy solution of this is of course to have some internal circuitry within the opamp to correct this input voltage.

So that moment circuit senses that there is some extra input voltage at the input it corrects it or there is some output voltage present there is some internal voltage itself generated which cancels this effect as if an external voltage is applied here something, so too just to mask the effect of this input voltage and internally generated voltage which is applied to the input that can correct this effect, but if we do not have that resource then a simple solution to that is to connect a capacitor in series with the resistance R1 like this.

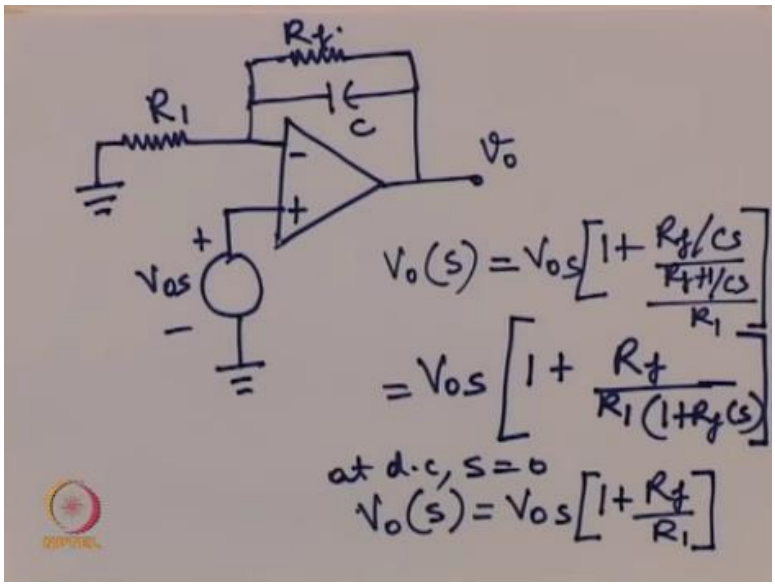
So, then the output voltage becomes something like this, so what you see is that when S = 0 that is at DC this Vo this is = Vos, S = 0. So what has changed on the previous case? When the output was given like this so this is now only Vos appears at the output there is no amplification, now this offset voltage is of a particular concern for integrated circuits the reason being in an integrator the circuit is given like this okay the output voltage for this configuration.

(Refer Slide Time: 05:32)



So this is the integrated circuit you have now have input offset voltage here, so this Vos will be given by Vos 1+1 upon CS upon R1 so this implies in the time domain this Vot will be given by Vos+Vos upon R1C times T, the very bad effect of this is as we can see from this equation is that as time progresses the output voltage keeps on increasing linearly with time which is a very dangerous effect, it might cause the output to get saturated by saturated I mean the output reaches its maximum value.

(Refer Slide Time: 07:22)

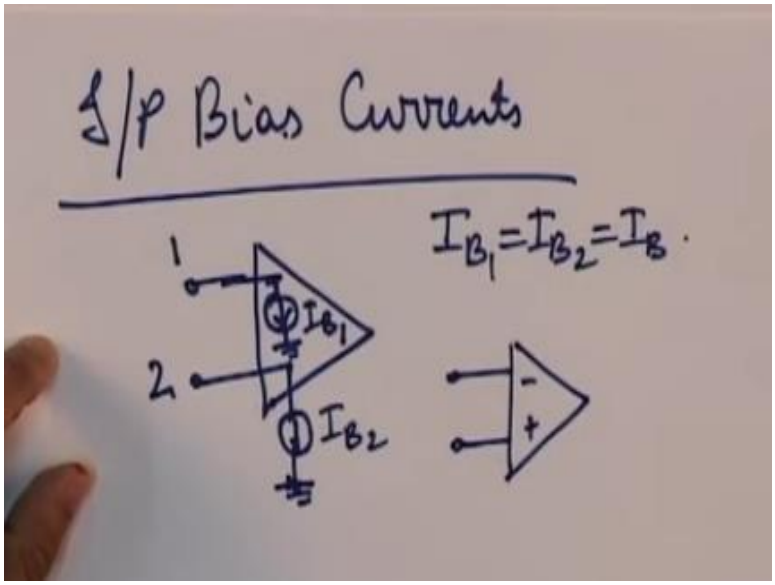


So to alleviate this problem or to at least ensure that output does not keep increasing linearly with time what is done is that if we have a resistance in shunt with the capacitor like this and by the way usually most capacitances have a certain Rf resistance in shunt so we do not always have

to explicitly add this resistance, so then what happens the Vos that is the output voltage it has an expression like this okay and this can be simplified to Vos 1+Rf upon R1 1+RfCS

Now at dc S is = 0 and this Vos becomes = Rf power, so at least you know the main problem in the previous case was that the output kept increasing linearly with time, now that will not happen of course there is a problem also here the problem is that this is not a perfect integrator anymore so that is a small problem but still it is at least the output does not get saturated.

(Refer Slide Time: 09:43)



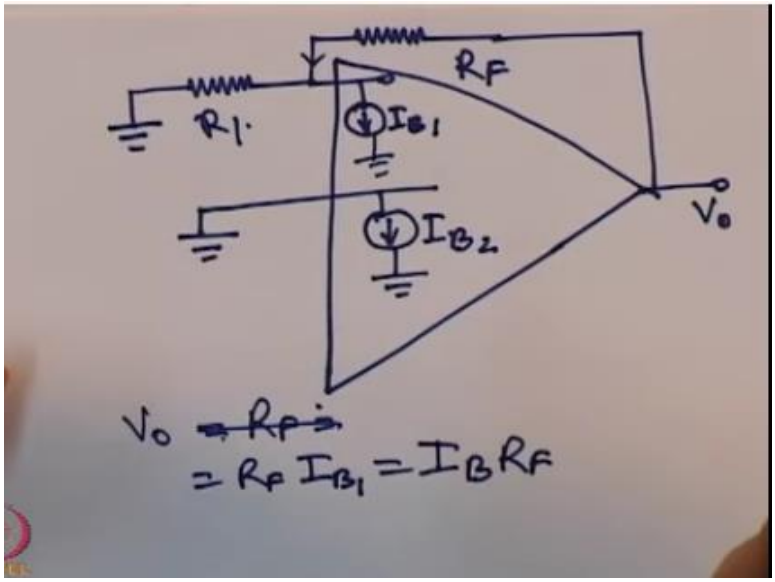
So one more problem that arises or one more non ideality that we are going to discuss is, what is known as bias currents or input bias current? So just like you are you know input offset voltage which is an undesirable input voltage appearing at the input of the opamp you might also have some undesirable bias current appearing at the input of the opamp.

So suppose you have an opamp like this, so you have 2 bias currents IB1 and IB2 and for the first case let us see the example when IB1 is = IB2 is = IBC say you have a inverting configuration let me describe this effect first so what you have is that any opamp for its operation needs certain input bias current.

Now we assume that as if the opamp when we discussed the opamp it was as if it was like this and then we added an AC signal by the way AC signal means any signal which is not DC usually

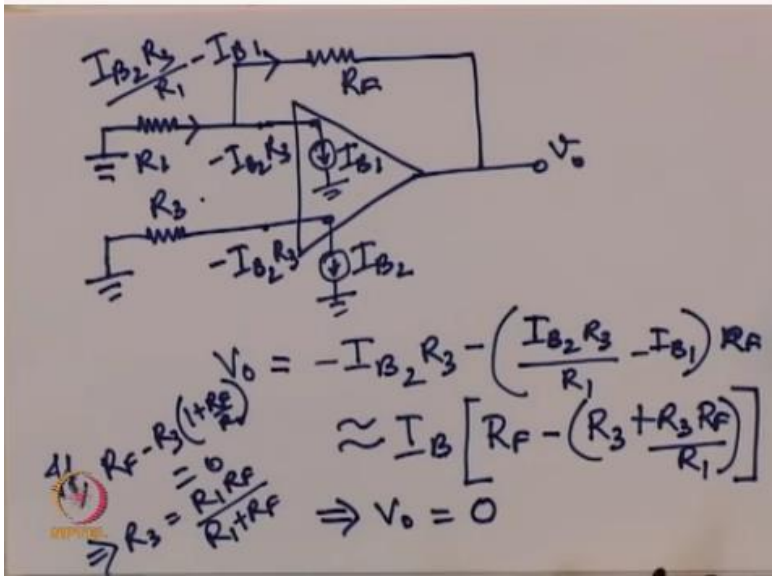
the signals that have to be amplified our AC signals, but then for its own operation it needs some DC bias current which is separate from the AC signal, now otherwise you know there is usually a separation between DC and AC components at the input but this DC bias currents that have been introduced have their own unique challenges.

(Refer Slide Time: 11:57)



Now once a challenge is that, let us see what happens if we have an inverting opamp little slightly expanded drawing of the opamp, so this is an opamp inverting configuration and your output Vo, without any input connected at this point will be given by RF is = sorry will be = R time IB1 which is = R IB2 RF, so because here no current is flowing to this resistance this IB1 has to flow through RF and therefore Vo must be at IB RF, so you see that the Vo input bias current is present then Vo will continue from a high level.

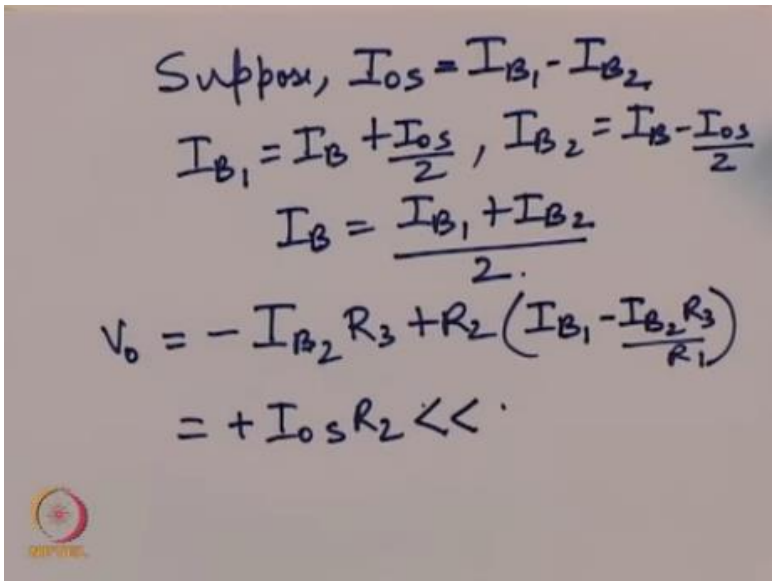
(Refer Slide Time: 13:50)



Now to get rid of this what can be done is we can introduce a resistance R3 in series with the non inverting input, so we have so the current flowing here is IB2 the voltage here is -IB2 R3 if the voltage is -IB2 R3 then it must be -IB2 R3 here as well the current flowing here is the current flowing through this -IB1 so therefore the current flowing is IB2R3 upon R1- IB1.

So then Vo is this voltage - the voltage drop across this resistance which is -IB2R3-IB2 R3 upon R1- IB1 time RF which is nearly = IB into RF - now if RF-R3 1+R upon R1 is = 0, then this implies R3 is = R1 R upon R1+R so if this condition is satisfied then this implies Vo will be = 0 so by suitable adjusting R3 we can ensure that Vo is = 0, of course here we are assuming one thing that these bias current IB1 and IB2 are the same.

(Refer Slide Time: 16:57)



Suppose they are not the same suppose there is a slight difference between the 2 bias currents, so then so suppose we have so then IB1 is given as IB+IB0S upon 2 and IB2 is = IB-Ios upon to here we have defined IB is = IB1+IB to call to ok then Vo will be given by using the same technique that I described earlier R2 which is = -Y+Ios R2 which is still a small quantity especially if we consider that the difference between IB1 and IB2 is very small it is usually the case then the output voltage due to the bias currents will still be very small.

So in this lecture, we covered 2 more non idealities related to opamps one was the OD offset voltage and the DC bias currents, both produce some undesirable effects as well this is more so for the DC especially very bad for the integrator case when the presence of a DC offset voltage caused the output to increase linearly with time and we also studied some of the methods to alleviate these problems in the next module.

We shall be covering what we call bode plots these are some important tools which are used to analyze the frequency response of various systems not just analog circuits and we shall see that these bode plots are an important tool they create is simplify the frequency analysis so that is what we will cover in the next lecture, thank you.